TDS-BD-APX500
Hardware User Manual

Rev.0.01

Revision History

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Table of Contents

1. Related Documents and Accessories 9
2. Overview 9
3. Feature 9
4. Block Diagram 10
5. External View of the Board 11
6. Board Specifications 12
7. Description of Components 13
7.1. Power Supply Structure 13
7.2. Clock Source 15
7.3. Jitter Attenuator 18
7.4. ADM Connector Interface 19
7.5. FMC Connector Interface 26
7.5.1. HPC Connector (High-Pin Count) 26
7.6. DDR3 SDRAM 31
7.7. PCI Express Edge 33
7.8. Analog Connector 36
7.9. Digital Connector 36
7.10. USB (UART) 37
7.11. LED 37
7.12. DIPSW 38
7.13. PushSW 39
7.14. Slide SW 39
7.15. External Power Supply Connector 40
7.16. Battery Control 40
8. Appendix 41
8.1. Creating a Configuration File 41
8.2. Writing a Configuration File into the Flash Memory 48
8.3. Configuration Time 53
9. Default Switch Settings 54
9.1. Figure 9-1 shows the default switch settings. 54

List of Figures

Figure 4-1 Block Diagram..... 10
Figure 5-1 Component Side..... 11
Figure 5-2 Solder Side..... 11
Figure 6-1 Board Dimensions (inclusive of wastable substrate)..... 12
Figure 7-1 Power Supply Structure..... 13
Figure 7-2 Power Supply Diagram..... 14
Figure 7-3 Power Status LED..... 14
Figure 7-4 Clock Sources..... 15
Figure 7-5 Clock Distribution Diagram..... 15
Figure 7-6 Internal Structure of Jitter Attenuator..... 18
Figure 7-7 ADM power LED..... 25
Figure 7-8 Cross-Point Structure..... 26
Figure 7-9 High-Pin Count Pinout..... 26
Figure 7-10 SDA, SCL, GA1/0 TDI/TDO Circuit..... 30
Figure 7-11 PG_C2M, PG_M2C, PRSNT_M2C_L Circuit Structure..... 30
Figure 7-12 VADJ Structure..... 30
Figure 7-13 DDR3-SDRAM Socket..... 31
Figure 7-14 PRSNT# Setting Structure..... 35
Figure 7-15 Power Supply from PCIE Edge..... 35
Figure 7-16 LED Structure..... 37
Figure 7-17 DIPSW Structure..... 38
Figure 7-18 PushSW Structure..... 39
Figure 7-19 Impedance Selection of External Signal..... 39
Figure 7-20 Program Chain Selection..... 40
Figure 7-21 External Power Supply Connector Structure..... 40
Figure 7-22 Battery Structure..... 40

List of Tables

Table 7-1 Power Status LED 14
Table 7-2 Details of Onboard Clock Sources 16
Table 7-3 Jitter Attenuator Setting Table 18
Table 7-4 F_SELx Function Setting Table 18
Table 7-5 ADM Connector Pinout(Component Side CN5) 19
Table 7-6 ADM Connector Pinout(Component Side CN4) 20
Table 7-7 ADM Connector Pinout(Mounting Side CN6) 22
Table 7-8 ADM Connector Pinout(Mounting Side CN7) 23
Table 7-9 HPC Connector Pinout Table 27
Table 7-10 DDR3 SO-DIMM Pinout Table 32
Table 7-11 PCI Express Edge Pinout Table 33
Table 7-12 PCI Express Lane Setting Table 35
Table 7-13 Feature of Analog Part 36
Table 7-14 Analog Connector Pinout Table 36
Table 7-15 Digital Connector Pinout Table 36
Table 7-16 UART Pinout Table 37
Table 7-17 LED Pinout Table 37
Table 7-18 DIPSW Pinout Table 38
Table 7-19 PushSW Pinout Table 39
Table 7-20 External Power Supply Connector Pinout Table 40

Introduction

Thank you for purchasing the **TDS-BD-APX500** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is a board intended for Xilinx FPGA, Virtex-6. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Board accessories:

- FMC spacer set

2. Overview

This board is the application board with Xilinx FPGA (Virtex6) LX130T/LX195T/LX240T. There are analog sample logic and digital processing logic on the board.

3. Feature

- PCI-Express BUS Interface Gen2(5Gbps) x8
- FPGA XC6VLX130T-FFG1156 (FFG1156 footprint device compatible)
- DDR3-SDRAM(SO-DIMM) PC3-12800 4GByte
- DDR3-SDRAM(Component) 1333MT/s 4Gbit
- SPI-FLASH(128Mbit) 50MHz
- ADM Connector x2
  - Data： LVDS 44pair 200MHz
  - Control： LVTTL 17pin 100MHz
  - Supply Power：+3.3V(1A) +6V(3A) -6V(1A)
- FMC Connector x1
  - Multi-gigabit signal：10pair 2.5GHz
  - Data+Clock signal：36pair 200MHz
  - Supply Power：+12V(1A) +2.5V(1A) +3.3V(4A)
- External USB-CN(UART)
- External Trigger-Input x1 (From ADM-Connector)
- External Trigger-Output x1 (From ADM-Connector)
- External Clock-Input x1 (From ADM-Connector)
- External Clock-Output x1 (From ADM-Connector)
- External Digital-Input x4
- External Digital-Output x4
- External Analog-Input x4 ±5V 16bit 250K sample
- External Analog-Ouput x4 ±5V or +5V 16bit output

- LOCAL-BUS signal 200MHz x 64bit
- Xilinx FPGA can be AES security protected
- 6pin ATX-CN +12V input

4. Block Diagram

Figure 4-1 provides a quick overview of the board block diagram.

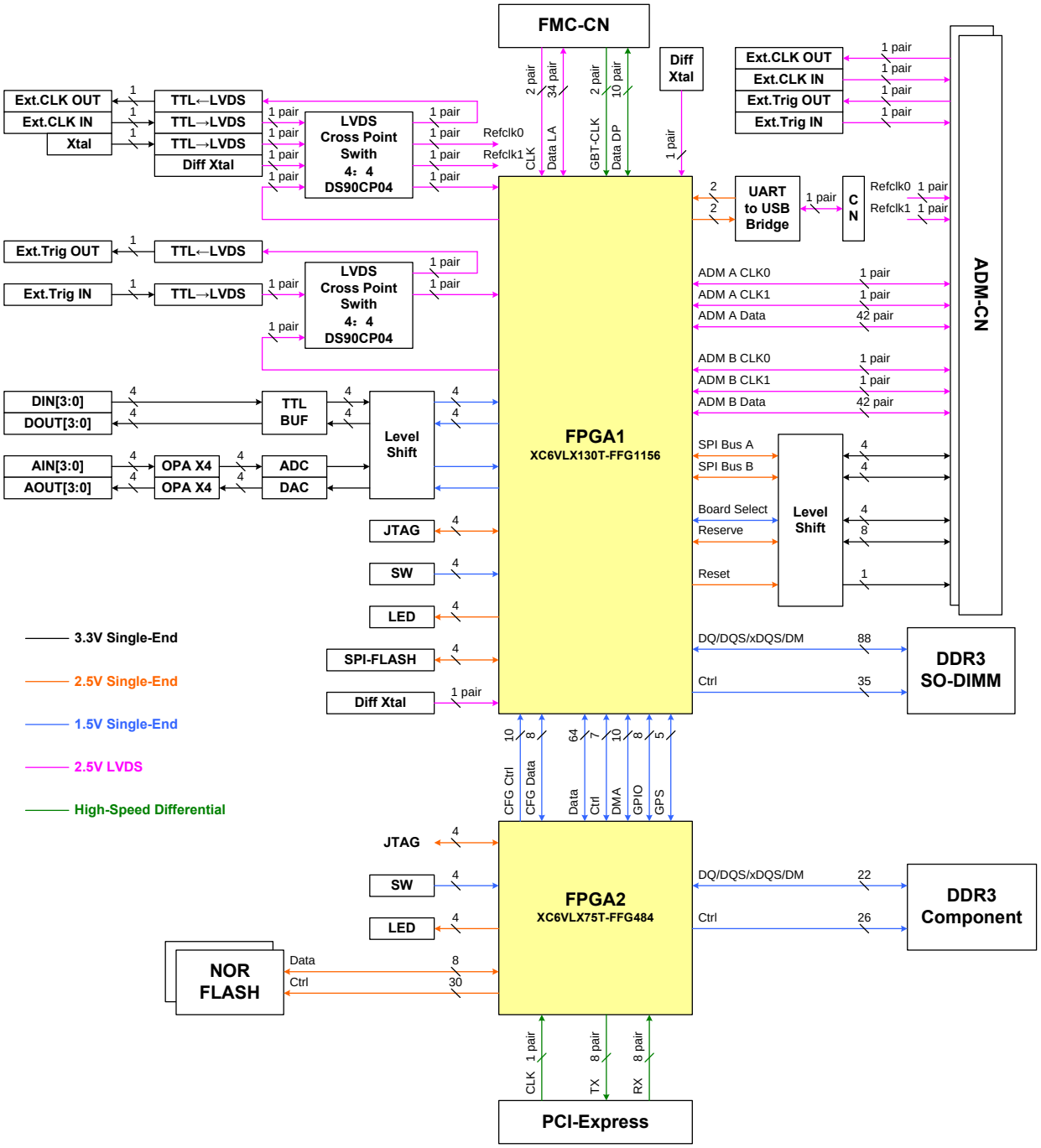


Figure 4-1 Block Diagram

5. External View of the Board

Figure 5-1 and 5-2 shows a board overview.

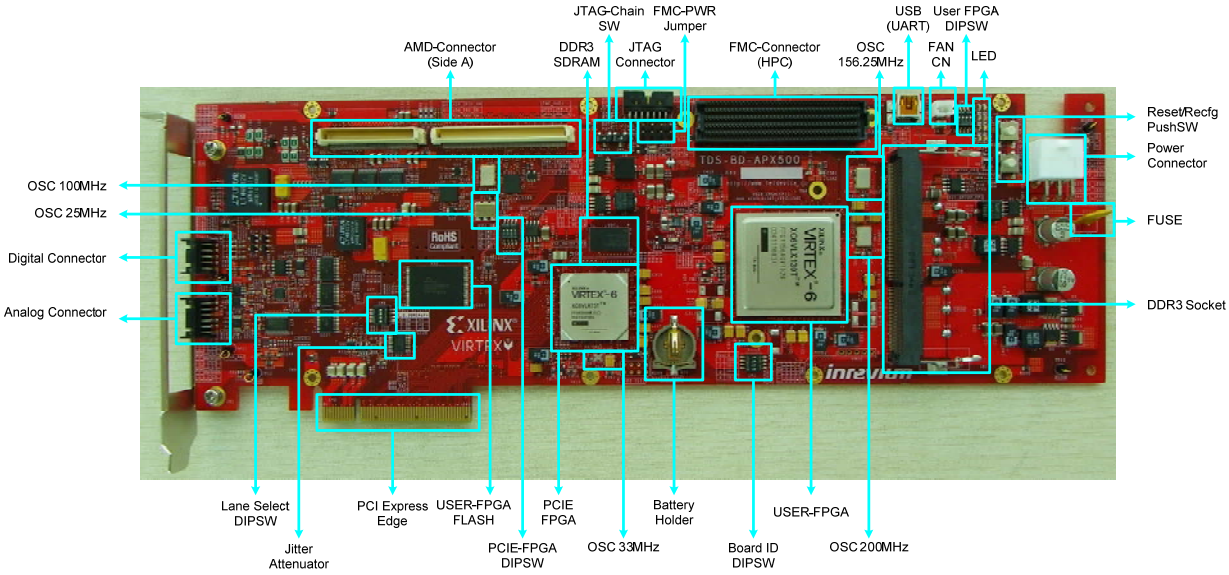


Figure 5-1 Component Side

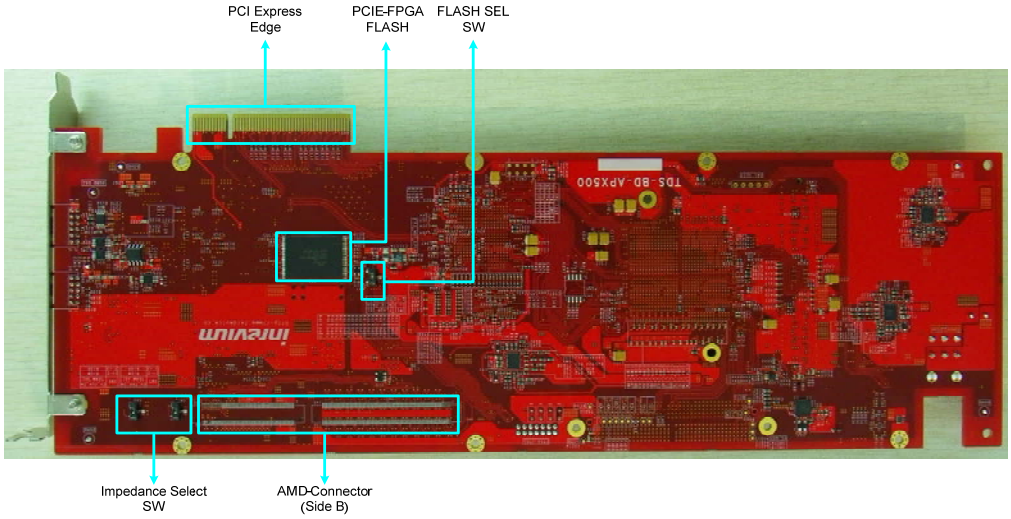


Figure 5-2 Solder Side

6. Board Specifications

Figure 6-1 shows the board specifications.

External Dimensions:	312.00 mm (W) x 111.15 mm (H)
Number of Layers:	12 layers
Board Thickness:	1.6 mm
Material:	FR-4
FPGA:	USER-FPGA: Xilinx XC6VLX130T-FFG1156
	PCIE-FPGA: Xilinx XC6VLX75T-FFG484
NOR-FLASH:	Spansion S29GL128P90TFIV1
SPI-FLASH:	Numonyx/ST M25PX16-VMW6TG
FMC Connector (High-Pin):	Samtec ASP-134486-01
ADM Connector	Hirose FX8C-100P-SV2(91)/ FX8C-140P-SV2(91)
DDR3 SDRAM:	ELPIDA EDJ1116DBSE-DJ-F
DDR3 SODIMM:	MT8JSF25664HZ-1G4
ADC 16-Bit 8-Channel:	ADI AD7689BCPZ
DAC 16-Bit Serial Input:	ADI AD5754RBREZ

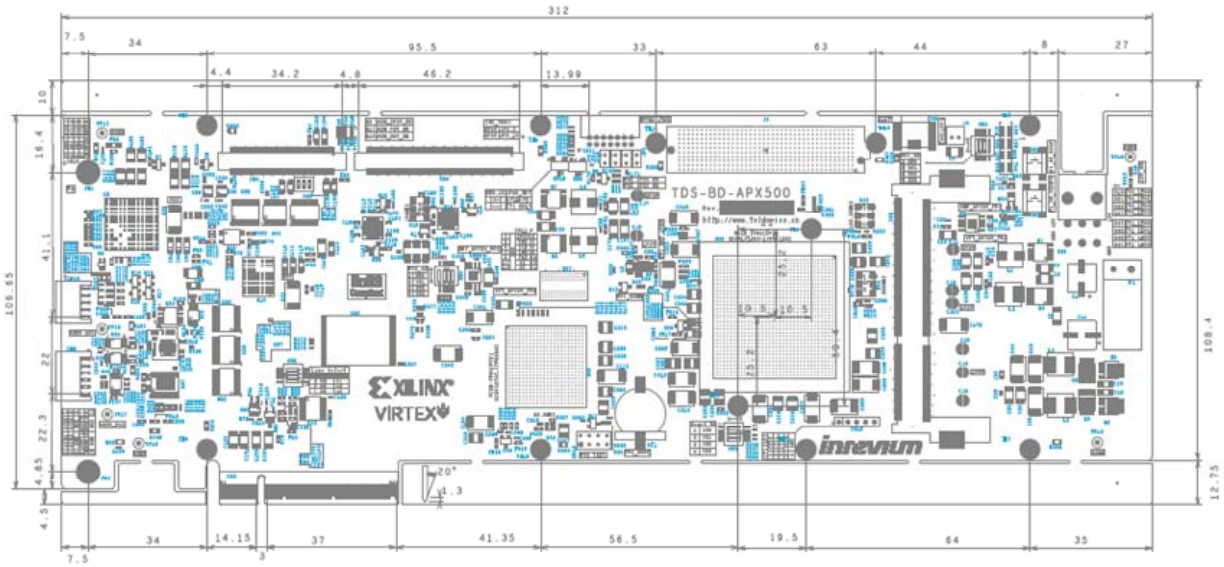


Figure 6-1 Board Dimensions (inclusive of wastable substrate)

7. Description of Components

7.1. Power Supply Structure

Figure 7-1 shows the internal power supply structure.

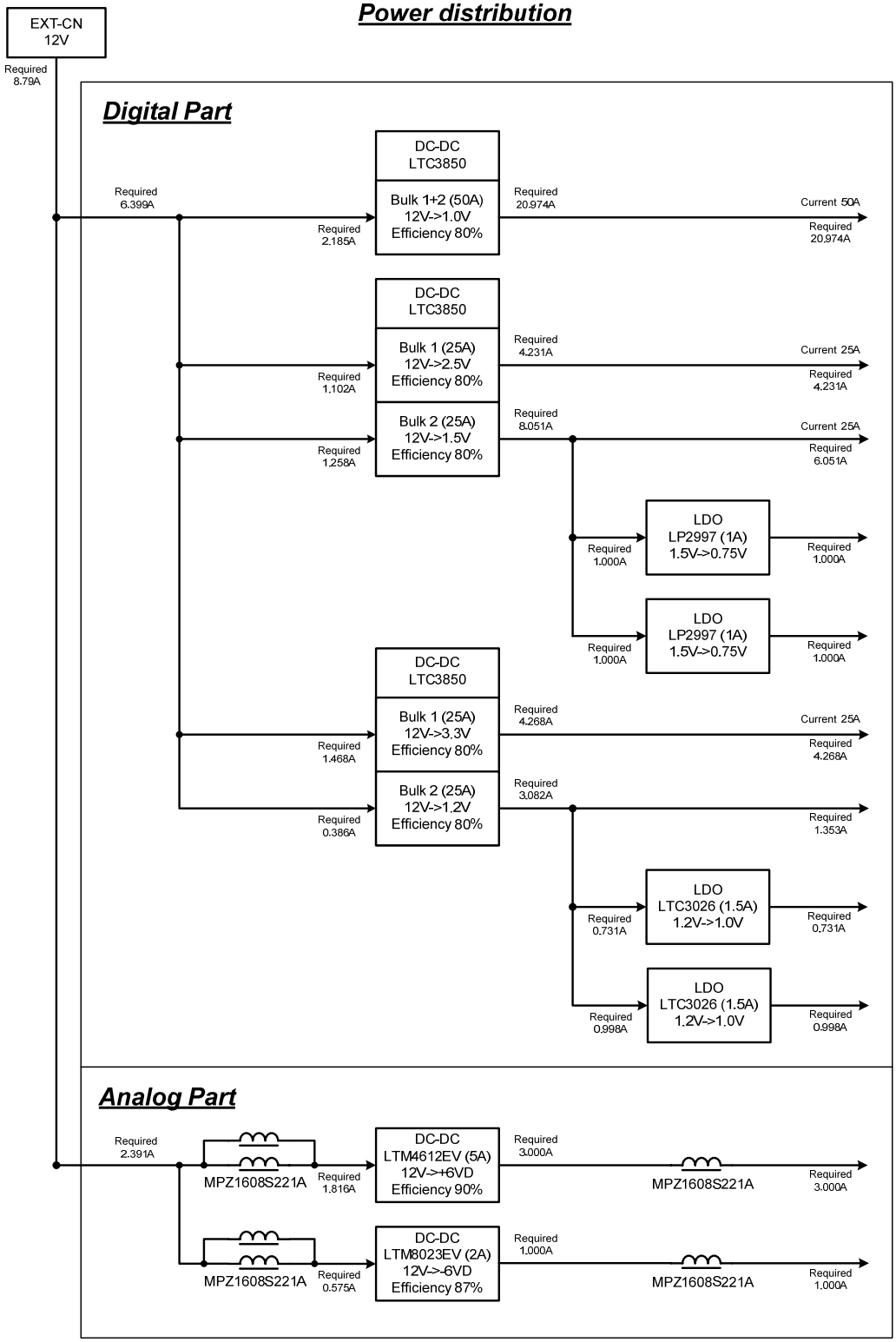


Figure 7-1 Power Supply Structure

Power Input

Power is supplied through the 12V ATX power supply connector.

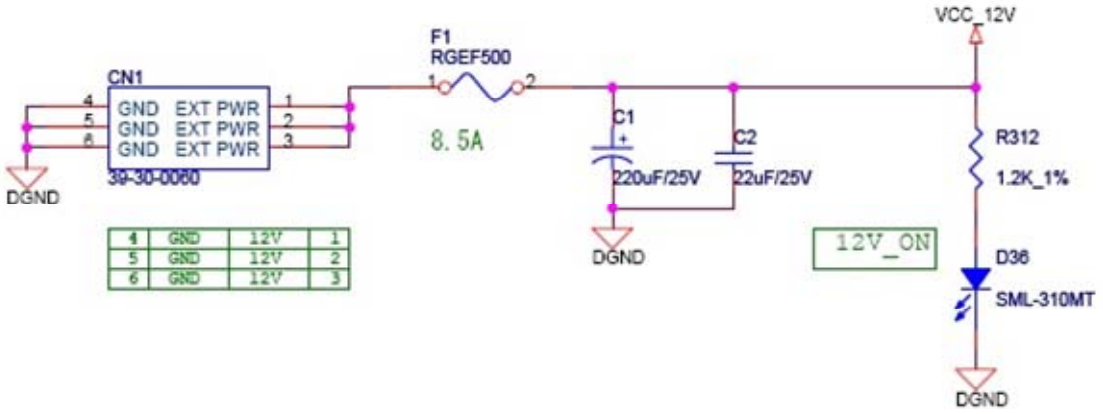


Figure 7-2 Power Supply Diagram

Power Status LED

The board provides 6 onboard LEDs to ensure the correct operation of power generation and distribution.

Table 7-1 Power Status LED

No.	LED No.	Voltage	Description	Color	Note
1	D9	+3.3V	+3.3V power supply on ADM-CN	Green	
2	D10	-6.0V	-6.0V power supply on ADM-CN	Green	
3	D11	+6.0V	+6.0V power supply on ADM-CN	Green	
4	D12	+2.5V	+2.5V(Vadj) power supply on FMC-CN	Green	
5	D13	+3.3V	+2.5V(Vadj) power supply on FMC-CN	Yellow	
6	D36	+12V	+12V power supply from ATX-CN	Green	

Figure 7-3 Power Status LED

7.2. Clock Source

The board provides the following clock sources.

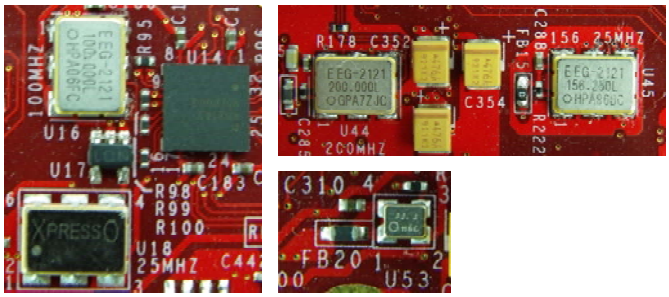


Figure 7-4 Clock Sources

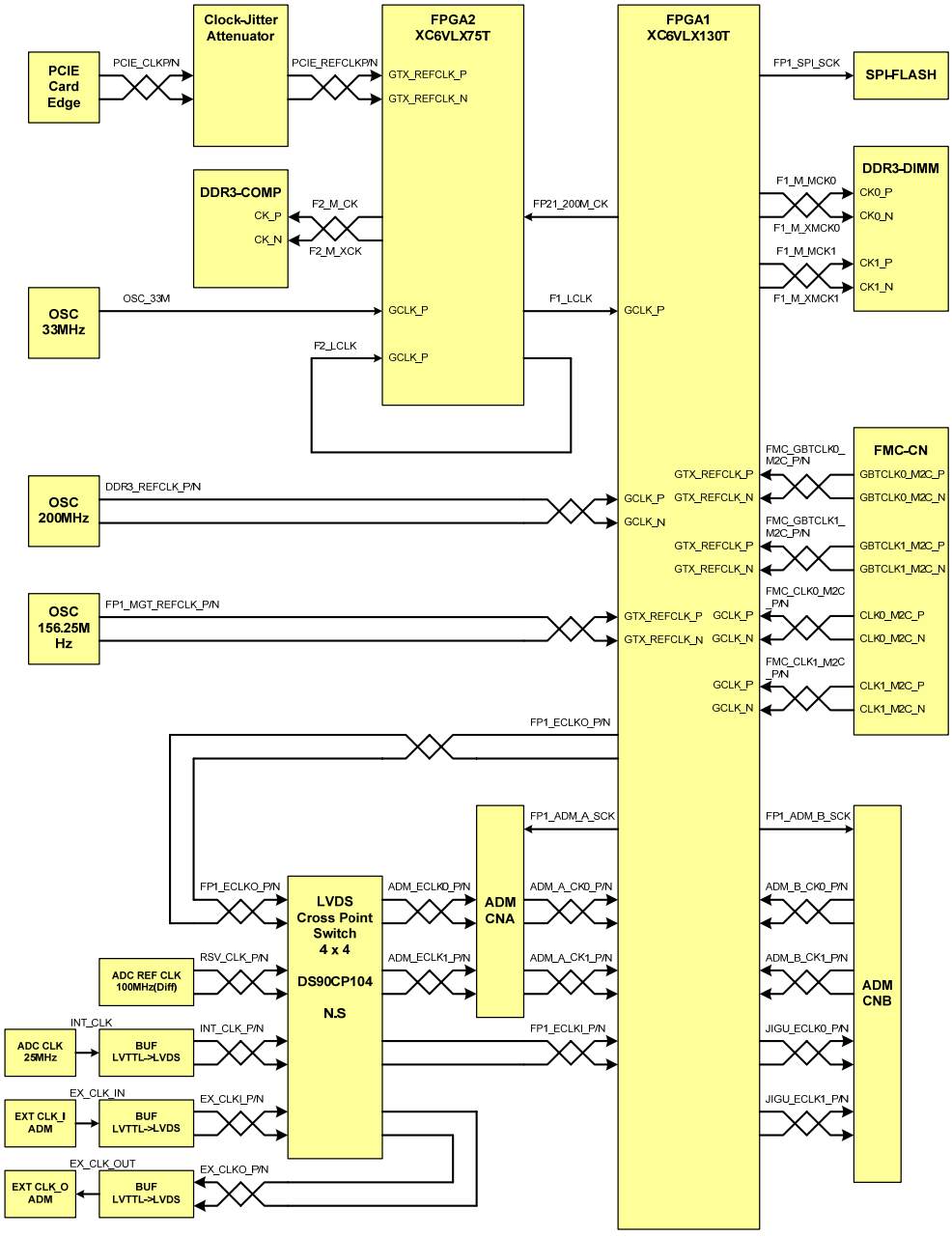


Figure 7-5 Clock Distribution Diagram

Table 7-2 shows the details of onboard clock sources.

Table 7-2 Details of Onboard Clock Sources

No.	Signal Name	Source		Destination			Remarks
		Device	No.	Device	No.	IO Standard	
1	PCIE_CLKP	CN2	A13	U12	12	CML	PCI Express clock from finger edge
2	PCIE_CLKN	CN2	A14	U12	13	CML	
3	PCIE_REFCLKP	U12	18	U48	L4	LVDS	PCI Express to FPGA
4	PCIE_REFCLKN	U12	17	U48	L3	LVDS	
5	DDR3_REFCLK_P	U44	4	U46	A10	LVDS	DDR3 (IDelay) clock
6	DDR3_REFCLK_N	U44	5	U46	B10	LVDS	
7	FP21_200M_CK	U46	D11	U48	F6	LVCMOS15	DDR3 clock for User FPGA
8	F1_M_MCK0	U46	B20	CN3	101	SSTL15	DDR3 DIMM Main clock 0
9	F1_M_XMCK0	U46	C19	CN3	103	SSTL15	
10	F1_M_MCK1	U46	C20	CN3	102	SSTL15	DDR3 DIMM Main clock 1
11	F1_M_XMCK1	U46	D20	CN3	104	SSTL15	
12	F2_M_CK	U48	E9	U57	J7	SSTL15	DDR3 Component Main clock
13	F2_M_XCK	U48	D9	U57	K7	SSTL15	
14	OSC_33M	U53	3	U48	T13	LVCMOS25	Main clock for User FPGA
15	FP1_LCLK	U48	E11	U46	K13	LVCMOS15	Local-bus clock for User FPGA
16	FP2_LCLK	U48	F11	U48	D12	LVCMOS15	Local-bus clock for PCIE FPGA
17	FP1_MGT_REFCLK_P	U45	4	U46	M6	LVDS	MGT Reference clock
18	FP1_MGT_REFCLK_N	U45	5	U46	M5	LVDS	
19	FMC_GBTCLK0_M2C_P	J1	D4	U46	P6	LVDS	MGT Reference clock from FMC-CN
20	FMC_GBTCLK0_M2C_N	J1	D5	U46	P5	LVDS	
21	FMC_GBTCLK1_M2C_P	J1	B20	U46	H6	LVDS	MGT Reference clock from FMC-CN
22	FMC_GBTCLK1_M2C_N	J1	B21	U46	H5	LVDS	
23	FMC_CLK0_M2C_P	J1	H4	U46	J9	LVDS	FMC interface clock
24	FMC_CLK0_M2C_N	J1	H5	U46	H9	LVDS	
25	FMC_CLK1_M2C_P	J1	G2	U46	L10	LVDS	FMC interface clock
26	FMC_CLK1_M2C_N	J1	G3	U46	M10	LVDS	
27	INT_CLK	U18	4	U17	5	LVTTL33	Oscillator clock(25MHz)
28	INT_CLK_P	U17	4	U14	16	LVDS	Via Single end to differential signal buffer
29	INT_CLK_N	U17	3	U14	15	LVDS	
30	RSV_CLK_P	U16	4	U14	14	LVDS	Oscillator clock(100Mhz Diff)
31	RSV_CLK_N	U16	5	U14	13	LVDS	
32	FP1_ECLKO_P	U46	AD30	U14	12	LVDS	External clock output from USER-FPGA
33	FP1_ECLKO_N	U46	AC30	U14	11	LVDS	
34	EX_CLK_IN	CN5	96	U13	5	LVTTL33	External clock input
35	EX_CLKI_P	U13	4	U14	10	LVDS	External clock input via

No.	Signal Name	Source		Destination			Remarks
		Device	No.	Device	No.	IO Standard	
36	EX_CLKI_N	U13	5	U14	9	LVDS	single end to differential signal buffer
37	EX_CLKO_P	U14	31	U15	3	LVDS	External clock output
38	EX_CLKO_N	U14	32	U15	4	LVDS	
39	EX_CLK_OUT	U15	5	CN5	92	LVTTL33	External clock output via single end to differential signal buffer
40	FP1_ECLKI_P	U14	29	U46	J25	LVDS	External clock output to USER-FPGA
41	FP1_ECLKI_N	U14	30	U46	J24	LVDS	
42	ADM_ECLK0_P	U14	27	CN4	1	LVDS	External clock to ADM-CN
43	ADM_ECLK0_N	U14	28	CN4	3	LVDS	
44	ADM_ECLK1_P	U14	25	CN4	2	LVDS	External clock to ADM-CN
45	ADM_ECLK1_N	U14	26	CN4	4	LVDS	
46	ADM_A_CK0_P	CN4	73	U46	AK27	LVDS	ADM interface clock(CH-A)
47	ADM_A_CK0_N	CN4	75	U46	AJ27	LVDS	
48	ADM_A_CK1_P	CN4	67	U46	L23	LVDS	ADM interface clock(CH-A)
49	ADM_A_CK1_N	CN4	69	U46	M22	LVDS	
50	FP1_ADM_A_SCK	U46	AD34	CN5	89	LVCMOS25	SPI-IF clock via ADM-CN
51	ADM_B_CK0_P	CN7	73	U46	AN27	LVDS	ADM interface clock(CH-B)
52	ADM_B_CK0_N	CN7	75	U46	AM27	LVDS	
53	ADM_B_CK1_P	CN7	67	U46	K24	LVDS	ADM interface clock(CH-B)
54	ADM_B_CK1_N	CN7	69	U46	K23	LVDS	
55	FP1_ADM_B_SCK	U46	AG31	CN6	89	LVCMOS25	SPI-IF clock via ADM-CN
56	JIGU_ECLK0_P	CN7	1	U46	U23	LVDS	External clock for test tool
57	JIGU_ECLK0_N	CN7	3	U46	V23	LVDS	
58	JIGU_ECLK1_P	CN7	2	U46	T24	LVDS	External clock for test tool
59	JIGU_ECLK1_N	CN7	4	U46	T23	LVDS	
60	FP1_SPI_SCK	U46	AJ11	U47	6	LVCMOS25	SPI interface clock

7.3. Jitter Attenuator

The board provides an onboard jitter attenuator generation circuit that uses IDT ICS874001AGI-05LF for PCI Express reference clock. For details about setting values, refer to the corresponding data sheet. Figure 7-6 shows the part of internal block diagram contained in the IDT ICS874001AGI-05LF data sheet.

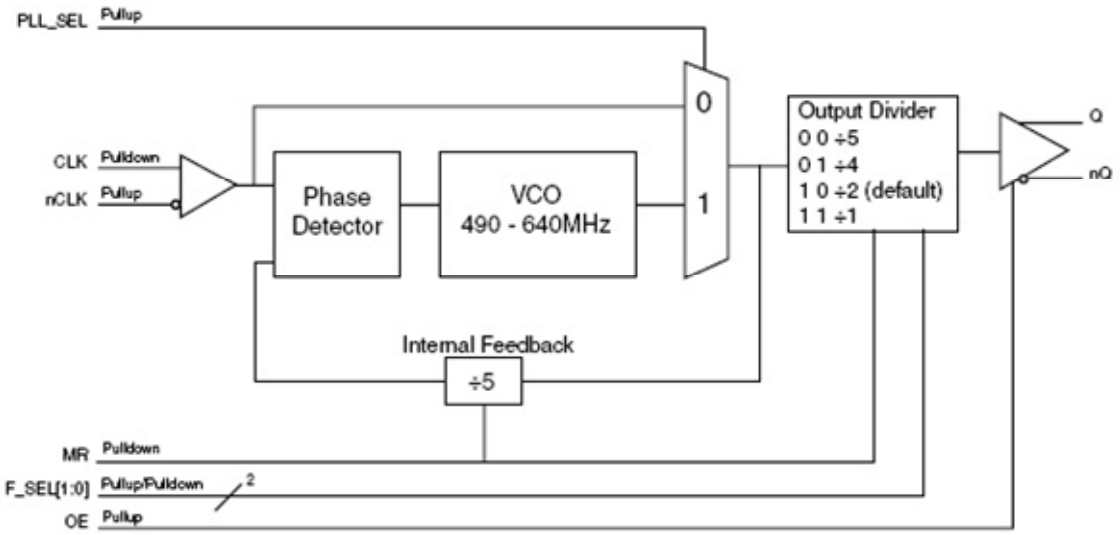


Figure 7-6 Internal Structure of Jitter Attenuator

The frequency of a clock generated by this PLL can be changed by setting the onboard resistors. This device connects clocks from the PCI Express Edge (A13/A14-pin). A reset to this device occurs during power-up.

Table 7-3 Jitter Attenuator Setting Table

Signal	Pull up	Pull down	Purpose
PLLSEL	*R83	R89	PLL select pin. (High = PLL enable/ Low = PLL bypass)
F_SEL1	*R85	R88	Frequency select pin. (Refer Table 7-xx)
F_SEL0	R84	*R87	Frequency select pin. (Refer Table 7-xx)
OE	*R86	-	Output clock enable (High = Enable)

* Default setting.

Table 7-4 F_SELx Function Setting Table

Inputs		Output Divider	Output Frequency Range (MHz)
F_SEL1	F_SEL0		
Low	Low	5	98 ~ 128
Low	High	4	122.5 ~ 160
High	Low	2	245 ~ 320 (Default)
High	High	1	490 ~ 640

7.4. ADM Connector Interface

The board provides 2 set ADM connectors for carrying the analog board of ADM-414. One set (CN4/CN5) is on component side, and the other one (CN6/CN7) is on mounting side. The ADM connector on the mounting side is not installed in the state of the factory shipment.

This connector is interfaced as follows:

Differential: 42-pairs (84 signals), 2-ch clocks and 2-ch external clocks

Single: 1-ch SPI-IF,1-ch ID set,1 pin reset, 2 pins clock,2 pins trigger and 8 pins reserves

Notice: Reserve pins, ID set pins and reset on component/mounting side are connected together

Table7-5 and Table 7-6 shows pinout of ADM connector on component side for User FPGA (U46).

Table 7-5 ADM Connector Pinout(Component Side CN5)

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		*1 3P3V	1	2	*1 N6V		
		*1 3P3V	3	4	*1 N6V		
		*1 3P3V	5	6	*1 N6V		
		*1 3P3V	7	8	*1 N6V		
		*1 3P3V	9	10	*1 N6V		
		*1 3P3V	11	12	*1 N6V		
		*1 3P3V	13	14	*1 N6V		
		*1 3P3V	15	16	*1 N6V		
		*1 3P3V	17	18	*1 N6V		
		*1 3P3V	19	20	*1 N6V		
			21	22			
			23	24			
		GND	25	26	*1 P6V		
		GND	27	28	*1 P6V		
		GND	29	30	*1 P6V		
		GND	31	32	*1 P6V		
		GND	33	34	*1 P6V		
		GND	35	36	*1 P6V		
		GND	37	38	*1 P6V		
		GND	39	40	*1 P6V		
		GND	41	42	*1 P6V		
		GND	43	44	*1 P6V		
		GND	45	46	*1 P6V		
		GND	47	48	*1 P6V		
		GND	49	50	*1 P6V		
		GND	51	52	*1 P6V		
		GND	53	54	*1 P6V		
		GND	55	56	*1 P6V		
		GND	57	58	*1 P6V		
		GND	59	60	*1 P6V		
		GND	61	62			
		GND	63	64			

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		GND	65	66	*4 RSV0	AA33	13
		GND	67	68	*4 RSV1	AB32	13
		GND	69	70	*4 RSV0	AB31	13
		GND	71	72	*4 RSV1	AC34	13
		GND	73	74	*4 RSV0	AB30	13
		GND	75	76	*4 RSV1	AC32	13
13	AE32	*2 BD_SEL0	77	78	*4 RSV0	AC33	13
13	AG31	*2 BD_SEL1	79	80	*4 RSV1	AD31	13
			81	82	PGND		
13	AF31	*2 BD_SEL2	83	84	*5 TRG_OUT		
13	AD32	*2 BD_SEL3	85	86	PGND		
			87	88	*5 TRG_IN		
13	AB33	*3 SCK	89	90	PGND		
13	AA30	*3 SDI	91	92	*5 CLK_OUT		
			93	94	PGND		
13	AE31	*3 SDO	95	96	*5 CLK_IN		
13	AA31	*3 SCS	97	98	PGND		
			99	100	*6 RSTN	AE34	13

Table 7-6 ADM Connector Pinout(Component Side CN4)

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		*5 ECLK0_P	1	2	*5 ECLK1_P		
		*5 ECLK0_N	3	4	*5 ECLK1_N		
		GND	5	6	GND		
22	AC20	LVDS_P40	7	8	LVDS_P41	AC15	32
22	AD20	LVDS_N40	9	10	LVDS_N41	AD15	32
		GND	11	12	GND		
32	AD17	LVDS_P38	13	14	LVDS_P39	AE16	32
32	AE17	LVDS_N38	15	16	LVDS_N39	AD16	32
		GND	17	18	GND		
22	AE21	LVDS_P36	19	20	LVDS_P37	AE18	32
22	AD21	LVDS_N36	21	22	LVDS_N37	AF18	32
		GND	23	24	GND		
22	AG20	LVDS_P34	25	26	LVDS_P35	AG15	32
22	AG21	LVDS_N34	27	28	LVDS_N35	AF15	32
		GND	29	30	GND		
32	AJ19	LVDS_P32	31	32	LVDS_P33	Y24	24
32	AH19	LVDS_N32	33	34	LVDS_N33	AA24	24
		GND	35	36	GND		
22	AJ20	LVDS_P30	37	38	LVDS_P31	AH25	23
22	AH20	LVDS_N30	39	40	LVDS_N31	AJ25	23

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		GND	41	42	GND		
24	AE23	LVDS_P28	43	44	LVDS_P29	AH17	32
24	AE22	LVDS_N28	45	46	LVDS_N29	AG17	32
		GND	47	48	GND		
22	AK22	LVDS_P26	49	50	LVDS_P27	AJ15	32
22	AJ22	LVDS_N26	51	52	LVDS_N27	AH15	32
		GND	53	54	GND		
23	AP25	LVDS_P24	55	56	LVDS_P25	AK14	32
23	AP24	LVDS_N24	57	58	LVDS_N25	AJ14	32
		GND	59	60	GND		
23	AG25	LVDS_P22	61	62	LVDS_P23	AK18	32
23	AG26	LVDS_N22	63	64	LVDS_N23	AK17	32
		GND	65	66	GND		
24	L23	LVDS_CK1_P	67	68	LVDS_P21	AM17	32
24	M22	LVDS_CK1_N	69	70	LVDS_N21	AM16	32
		GND	71	72	GND		
23	AK27	LVDS_CK0_P	73	74	LVDS_P20	AN15	32
23	AJ27	LVDS_CK0_N	75	76	LVDS_N20	AM15	32
		GND	77	78	GND		
24	AA23	LVDS_P18	79	80	LVDS_P19	AL16	32
24	AB23	LVDS_N18	81	82	LVDS_N19	AK16	32
		GND	83	84	GND		
32	AC18	LVDS_P16	85	86	LVDS_P17	AM18	22
32	AC17	LVDS_N16	87	88	LVDS_N17	AL18	22
		GND	89	90	GND		
32	AN17	LVDS_P14	91	92	LVDS_P15	AP19	22
32	AP17	LVDS_N14	93	94	LVDS_N15	AN18	22
		GND	95	96	GND		
32	AG16	LVDS_P12	97	98	LVDS_P13	AF19	22
32	AF16	LVDS_N12	99	100	LVDS_N13	AE19	22
		GND	101	102	GND		
24	AC22	LVDS_P10	103	104	LVDS_P11	AM21	22
24	AD22	LVDS_N10	105	106	LVDS_N11	AL21	22
		GND	107	108	GND		
22	AM20	LVDS_P8	109	110	LVDS_P9	AM22	22
22	AL20	LVDS_N8	111	112	LVDS_N9	AN22	22
		GND	113	114	GND		
23	AH23	LVDS_P6	115	116	LVDS_P7	AP22	22
23	AH24	LVDS_N6	117	118	LVDS_N7	AN23	22
		GND	119	120	GND		
12	AG27	LVDS_P4	121	122	LVDS_P5	AN25	23
12	AG28	LVDS_N4	123	124	LVDS_N5	AN24	23
		GND	125	126	GND		
12	AE28	LVDS_P2	127	128	LVDS_P3	AC23	24

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
12	AE29	LVDS_N2	129	130	LVDS_N3	AC24	24
		GND	131	132	GND		
12	AE27	LVDS_P0	133	134	LVDS_P1	AF26	12
12	AD27	LVDS_N0	135	136	LVDS_N1	AE26	12
		GND	137	138	GND		
		GND	139	140	GND		

Table7-7 and Table 7-8 show pinout of ADM connector on mounting side for User FPGA (U46).

Table 7-7 ADM Connector Pinout(Mounting Side CN6)

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		*1 3P3V	1	2	*1 N6V		
		*1 3P3V	3	4	*1 N6V		
		*1 3P3V	5	6	*1 N6V		
		*1 3P3V	7	8	*1 N6V		
		*1 3P3V	9	10	*1 N6V		
		*1 3P3V	11	12	*1 N6V		
		*1 3P3V	13	14	*1 N6V		
		*1 3P3V	15	16	*1 N6V		
		*1 3P3V	17	18	*1 N6V		
		*1 3P3V	19	20	*1 N6V		
			21	22			
			23	24			
		GND	25	26	*1 P6V		
		GND	27	28	*1 P6V		
		GND	29	30	*1 P6V		
		GND	31	32	*1 P6V		
		GND	33	34	*1 P6V		
		GND	35	36	*1 P6V		
		GND	37	38	*1 P6V		
		GND	39	40	*1 P6V		
		GND	41	42	*1 P6V		
		GND	43	44	*1 P6V		
		GND	45	46	*1 P6V		
		GND	47	48	*1 P6V		
		GND	49	50	*1 P6V		
		GND	51	52	*1 P6V		
		GND	53	54	*1 P6V		
		GND	55	56	*1 P6V		
		GND	57	58	*1 P6V		
		GND	59	60	*1 P6V		
		GND	61	62			

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		GND	63	64			
		GND	65	66	*4 RSV0	AA33	13
		GND	67	68	*4 RSV1	AB32	13
		GND	69	70	*4 RSV0	AB31	13
		GND	71	72	*4 RSV1	AC34	13
		GND	73	74	*4 RSV0	AB30	13
		GND	75	76	*4 RSV1	AC32	13
13	AE32	*2 BD_SEL0	77	78	*4 RSV0	AC33	13
13	AG31	*2 BD_SEL1	79	80	*4 RSV1	AD31	13
			81	82	PGND		
13	AF31	*2 BD_SEL2	83	84	*6 TRG_OUT	V30	14
13	AD32	*2 BD_SEL3	85	86	PGND		
			87	88	*6 TRG_IN	W30	14
13	AA34	*3 SCK	89	90	PGND		
13	AA29	*3 SDI	91	92	*6 CLK_OUT	W34	14
			93	94	PGND		
13	AD34	*3 SDO	95	96	*6 CLK_IN	V34	14
13	AA28	*3 SCS	97	98	PGND		
			99	100	*6 RSTN	AE34	13

Table 7-8 ADM Connector Pinout(Mounting Side CN7)

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
		*5 ECLK0_P	1	2	*5 ECLK1_P		
		*5 ECLK0_N	3	4	*5 ECLK1_N		
		GND	5	6	GND		
32	AP16	LVDS_P40	7	8	LVDS_P41	AM23	22
32	AP15	LVDS_N40	9	10	LVDS_N41	AL23	22
		GND	11	12	GND		
22	AN19	LVDS_P38	13	14	LVDS_P39	AG22	23
22	AN20	LVDS_N38	15	16	LVDS_N39	AH22	22
		GND	17	18	GND		
24	AF23	LVDS_P36	19	20	LVDS_P37	AM25	23
24	AG23	LVDS_N36	21	22	LVDS_N37	AL25	23
		GND	23	24	GND		
22	AP20	LVDS_P34	25	26	LVDS_P35	AK21	22
22	AP21	LVDS_N34	27	28	LVDS_N35	AJ21	22
		GND	29	30	GND		
22	AF20	LVDS_P32	31	32	LVDS_P33	AP27	23
22	AF21	LVDS_N32	33	34	LVDS_N33	AP26	23
		GND	35	36	GND		
23	AK23	LVDS_P30	37	38	LVDS_P31	AL26	23

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
23	AL24	LVDS_N30	39	40	LVDS_N31	AM26	23
		GND	41	42	GND		
32	AH18	LVDS_P28	43	44	LVDS_P29	AN28	23
32	AG18	LVDS_N28	45	46	LVDS_N29	AM28	23
		GND	47	48	GND		
23	AK26	LVDS_P26	49	50	LVDS_P27	AL30	12
23	AJ26	LVDS_N26	51	52	LVDS_N27	AM31	12
		GND	53	54	GND		
22	AK19	LVDS_P24	55	56	LVDS_P25	AJ31	12
22	AL19	LVDS_N24	57	58	LVDS_N25	AJ32	12
		GND	59	60	GND		
12	AD25	LVDS_P22	61	62	LVDS_P23	AN30	23
12	AD26	LVDS_N22	63	64	LVDS_N23	AM30	23
		GND	65	66	GND		
24	K24	LVDS_CK1_P	67	68	LVDS_P21	AK33	12
24	K23	LVDS_CK1_N	69	70	LVDS_N21	AK32	12
		GND	71	72	GND		
23	AN27	LVDS_CK0_P	73	74	LVDS_P20	AN32	12
23	AM27	LVDS_CK0_N	75	76	LVDS_N20	AM32	12
		GND	77	78	GND		
32	AJ17	LVDS_P18	79	80	LVDS_P19	AJ24	23
32	AJ16	LVDS_N18	81	82	LVDS_N19	AK24	23
		GND	83	84	GND		
23	AL29	LVDS_P16	85	86	LVDS_P17	AL28	23
23	AK29	LVDS_N16	87	88	LVDS_N17	AK28	23
		GND	89	90	GND		
32	AL15	LVDS_P14	91	92	LVDS_P15	AL34	12
32	AL14	LVDS_N14	93	94	LVDS_N15	AK34	12
		GND	95	96	GND		
23	AN29	LVDS_P12	97	98	LVDS_P13	AJ29	12
23	AP29	LVDS_N12	99	100	LVDS_N13	AJ30	12
		GND	101	102	GND		
22	AC19	LVDS_P10	103	104	LVDS_P11	AL31	12
22	AD19	LVDS_N10	105	106	LVDS_N11	AK31	12
		GND	107	108	GND		
23	AP30	LVDS_P8	109	110	LVDS_P9	AH29	12
23	AP31	LVDS_N8	111	112	LVDS_N9	AH30	12
		GND	113	114	GND		
23	AH27	LVDS_P6	115	116	LVDS_P7	AM33	12
23	AH28	LVDS_N6	117	118	LVDS_N7	AL33	12
		GND	119	120	GND		
12	AF28	LVDS_P4	121	122	LVDS_P5	AN33	12
12	AF29	LVDS_N4	123	124	LVDS_N5	AN34	12
		GND	125	126	GND		

FPGA		ADM Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
12	AP32	LVDS_P2	127	128	LVDS_P3	AF30	12
12	AP33	LVDS_N2	129	130	LVDS_N3	AG30	12
		GND	131	132	GND		
12	AJ34	LVDS_P0	133	134	LVDS_P1	AH33	12
12	AH34	LVDS_N0	135	136	LVDS_N1	AH32	12
		GND	137	138	GND		
		GND	139	140	GND		

*** 1 Power Supply**

The board provides +6V output to the P6V pin and -6V output to the N6V pins. 3.3V outputs are also provided to the 3P3V pins. The power status can be monitored by the adjacent LED.

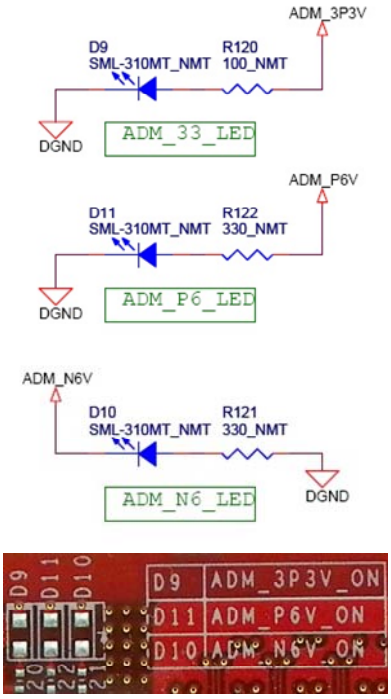


Figure 7-7 ADM power LED

***2 BD_SEL[3:0]**

The board provides the board ID setting signal to the carrier board. User can set the board ID of the carrier board though these pins by FPGA design.

***3 SCK, SCS, SDI, SDO**

The board provides a SPI interface for accessing the device on carrier board for each connector. User can set the parameter and read the status of the device on the carrier board though these pins by FPGA design.

***4 RSV[7:0]**

The board provides reserve pins for expansion in future.

***5 ECLK0_P/N, ECLK1_P/N, TRG_IN, TRG_OUT, CLK_IN, CLK_OUT (Component side)**

The board provides the external clock and trigger output pins to carrier board. The external clocks and triggers can be selected by setting the cross-point device on this board. User can set the function by FPGA design. Please make caution to the pins named MODE, LOAD, SI/SEL1, SCLK, SEL0.

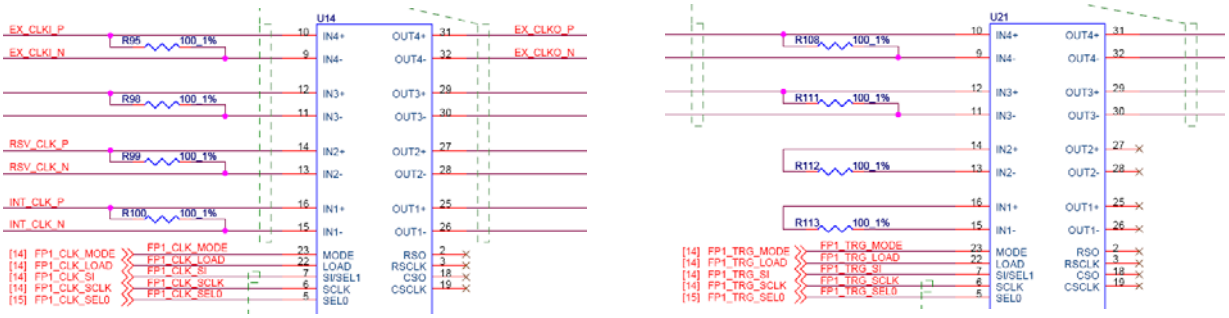


Figure 7-8 Cross-Point Structure

***6 RSTN, TRG_IN, TRG_OUT, CLK_IN, CLK_OUT (Mounting side)**

The board provides the reset signal, trigger signal and clock signal for the control communication between this board and the carrier board. User can set the pins by FPGA design.

7.5. FMC Connector Interface

The board provides a Samtec FMC High-Pin Count (J1) connectors.

Figure 7-9 show High-Pin Count pinout respectively.

Notice: All pins of HPC are not connected to the FPGA.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-9 High-Pin Count Pinout

7.5.1. HPC Connector (High-Pin Count)

The board uses a High-Pin Count connector. Due considerations to the number of FPGA pins, the column of E, F, J, K pins are not connected. This connector is interfaced as follows:

High Speed: 10-ch TX, 10-ch RX and 2-ch clocks

Low Speed: 34-pairs (68 signals) and 2-ch clocks

Table7-9 shows a HPC connector pinout for User FPGA (U46).

Table 7-9 HPC Connector Pinout Table

Bank No.	Pin No.	A		B	Pin No.	Bank No.
		GND	1	RES1		
MGTRXP2_116	D5	DP1_M2C_P	2	GND		
MGTRXN2_116	D6	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	E3	MGTRXP1_116
		GND	5	DP9_M2C_N	E4	MGTRXN1_116
MGTRXP0_116	G3	DP2_M2C_P	6	GND		
MGTRXN0_116	G4	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	J3	MGTRXP3_115
		GND	9	DP8_M2C_N	J4	MGTRXN3_115
MGTRXP2_115	K5	DP3_M2C_P	10	GND		
MGTRXN2_115	K6	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	L3	MGTRXP1_115
		GND	13	DP7_M2C_N	L4	MGTRXN1_115
MGTRXP0_115	N3	DP4_M2C_P	14	GND		
MGTRXN0_115	N4	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	R3	MGTRXP3_114
		GND	17	DP6_M2C_N	R4	MGTRXN3_114
MGTRXP2_114	U3	DP5_M2C_P	18	GND		
MGTRXN2_114	U4	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	H6	MGTREFCLK0P_116
		GND	21	*1 GBTCLK1_M2C_N	H5	MGTREFCLK0N_116
MGTTXP2_116	B1	DP1_C2M_P	22	GND		
MGTTXN2_116	B2	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	C3	MGTTXP1_116
		GND	25	DP9_C2M_N	C4	MGTTXN1_116
MGTTXP0_116	D1	DP2_C2M_P	26	GND		
MGTTXN0_116	D2	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	F1	MGTTXP3_115
		GND	29	DP8_C2M_N	F2	MGTTXN3_115
MGTTXP2_115	H1	DP3_C2M_P	30	GND		
MGTTXN2_115	H2	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	K1	MGTTXP1_115
		GND	33	DP7_C2M_N	K2	MGTTXN1_115
MGTTXP0_115	M1	DP4_C2M_P	34	GND		
MGTTXN0_115	M2	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	P1	MGTTXP3_114
		GND	37	DP6_C2M_N	P2	MGTTXN3_114
MGTTXP2_114	T1	DP5_C2M_P	38	GND		
MGTTXN2_114	T2	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*5 PG_C2M		
MGTTXP3_116	A3	DP0_C2M_P	2	GND		
MGTTXN3_116	A4	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	P6	MGTREFCLK0P_115
		GND	5	*1 GBTCLK0_M2C_N	P5	MGTREFCLK0N_115
MGTRXP3_116	B5	DP0_M2C_P	6	GND		
MGTRXN3_116	B6	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	L9	34
		GND	9	LA01_N_CC	K9	34
34	B8	LA06_P	10	GND		
34	C8	LA06_N	11	LA05_P	AD10	34
		GND	12	LA05_N	AC9	34
		GND	13	GND		
34	AF9	LA10_P	14	LA09_P	F9	34
34	AF10	LA10_N	15	LA09_N	F10	34
		GND	16	GND		
		GND	17	LA13_P	AK9	34
34	AK8	LA14_P	18	LA13_N	AL9	34
34	AL8	LA14_N	19	GND		
		GND	20	LA17_P_CC	AC13	33
		GND	21	LA17_N_CC	AC12	33
33	AD12	LA18_P_CC	22	GND		
33	AD11	LA18_N_CC	23	LA23_P	AF13	33
		GND	24	LA23_N	AG13	33
		GND	25	GND		
33	AG12	LA27_P	26	LA26_P	AJ10	33
33	AH12	LA27_N	27	LA26_N	AH10	33
		GND	28	GND		
		GND	29	TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*3 GA0	34	TRST_L		
		*6 12P0V	35	*3 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*5 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*7 VREF_A_M2C		
34	L10	CLK1_M2C_P	2	*5 PRSNT_M2C_L		
34	M10	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	J9	34
		GND	5	CLK0_M2C_N	H9	34
34	AC10	LA00_P_CC	6	GND		
34	AB10	LA00_N_CC	7	LA02_P	A9	34
		GND	8	LA02_N	A8	34
34	C10	LA03_P	9	GND		
34	D10	LA03_N	10	LA04_P	C9	34
		GND	11	LA04_N	D9	34
34	E8	LA08_P	12	GND		
34	E9	LA08_N	13	LA07_P	AD9	34
		GND	14	LA07_N	AE9	34
34	AG8	LA12_P	15	GND		
34	AH8	LA12_N	16	LA11_P	AH9	34
		GND	17	LA11_N	AJ9	34
34	AN10	LA16_P	18	GND		
34	AP10	LA16_N	19	LA15_P	AN9	34
		GND	20	LA15_N	AP9	34
33	AH13	LA20_P	21	GND		
33	AH14	LA20_N	22	LA19_P	AE14	33
		GND	23	LA19_N	AF14	33
33	AF11	LA22_P	24	GND		
33	AE11	LA22_N	25	LA21_P	AG11	33
		GND	26	LA21_N	AG10	33
33	AK12	LA25_P	27	GND		
33	AJ12	LA25_N	28	LA24_P	AK13	33
		GND	29	LA24_N	AL13	33
33	AM10	LA29_P	30	GND		
33	AL10	LA29_N	31	LA28_P	AL11	33
		GND	32	LA28_N	AM11	33
33	AM12	LA31_P	33	GND		
33	AN12	LA31_N	34	LA30_P	AP11	33
		GND	35	LA30_N	AP12	33
33	AN13	LA33_P	36	GND		
33	AM13	LA33_N	37	LA32_P	AP14	33
		GND	38	LA32_N	AN14	33
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

*** 1 GBTCLK0_M2C_P/N**

This signal is used for reference clock of MGT. But it is needs to select this clock or 156.25MHz Oscillator.

*** 2 SCL, SDA**

The board provides test points PAD to enable I2C communications with the FMC mezzanine card.

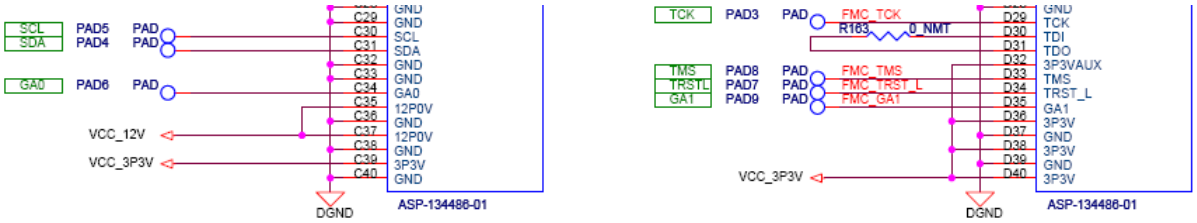


Figure 7-10 SDA, SCL, GA1/0, TDI/TDO Circuit

*** 3 GA[1:0]**

The board provides test points PAD for notification of an ID to the FMC mezzanine card.

*** 4 TDI, TDO**

The board provides a loopback structure for JTAG communication from the FMC mezzanine card. By default, this loopback function is not provided because the R163 resistor is not installed.

*** 5 PG_C2M, PG_M2C, PRSNT_M2C_L**

The board provides test points PAD and pull-up resistor to output to the FMC mezzanine card. It also provides a similar structure for the column of F pins of the FMC connector. The PG_M2C, PRSNT_M2C_L also has a similar structure.

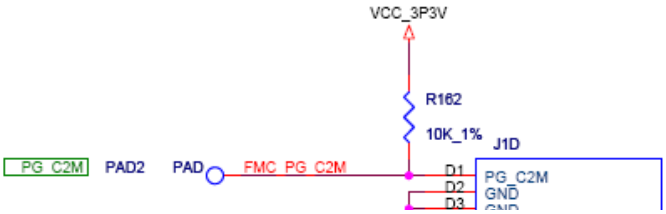


Figure 7-11 PG_C2M, PG_M2C, PRSNT_M2C_L Circuit Structure

*** 6 Power Supply**

The board provides 12V output to the 12P0V pin and 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The target pins are E39 and F40. The voltage supply can be provided by short-circuiting one portion of JP4, 5 and JP9, 10 respectively. The power status can be monitored by the adjacent LED.

Caution:

Do not short-circuit JP4 and JP9 on the same time, and also JP5 and JP10.

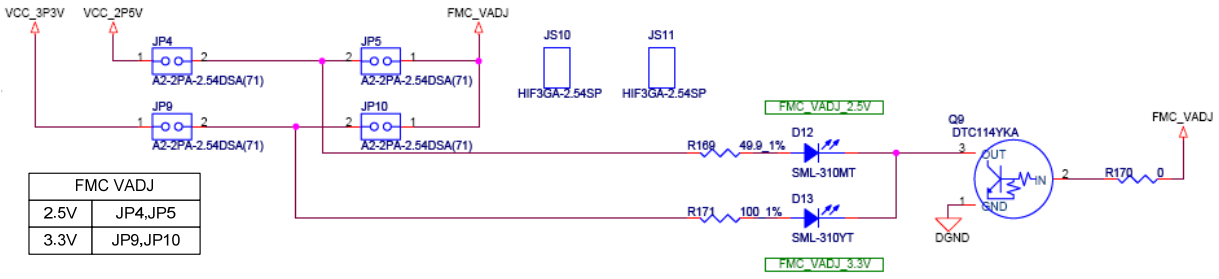


Figure 7-12 VADJ Structure

***7 VREF_A_M2C, VREF_B_M2C**

The VREF_A_M2C terminal of the H1 pin can be monitored by PAD12 and the VREF_B_M2C terminal of the K1 pin by PAD13.

***8 VIO_B_M2C**

The VIO_B_M2C terminal of each J39 and K40 pin can be monitored by PAD14.

7.6. DDR3 SDRAM

The board provides one DDR3 SODIMM socket for User FPGA (U46).

The following pins are connected:

A[14:0], DQ[63:0], ODT[1:0], DQS[7:0], xDQS[7:0], DM[7:0], CK[1:0], xCK[1:0], CKE[1:0], xRAS, xCAS, xWE, xCS[1:0] and BA[2:0]

A[14], are a memory address expansion bit.

The board comes with a 1GB DDR3 so-dimm using A[13:0].

Specifications

1GB(128Mword x 8bit x 8bank)

1066(7-7-7)

Address Structure

Bank=3bit

Address=14bit (Row address=14bit / Column address=10bit)

Data Bus Structure

Per-byte data strobe with write and read DQS

Per-byte data mask (DM)

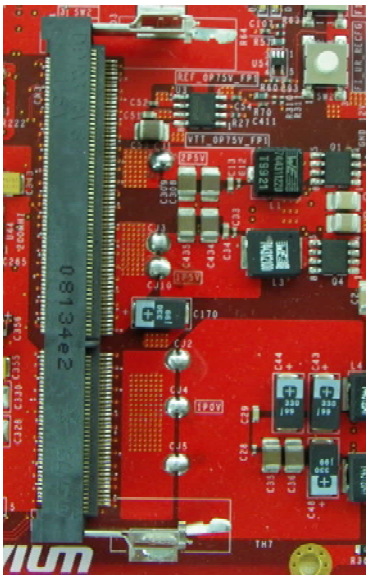


Figure 7-13 DDR3-SDRAM Socket

Table 7-10 DDR3 SO-DIMM Pinout Table

DDR2 Pin Name	FPGA	
	Pin No.	IO Standard
ODT0	A19	SSTL15
ODT1	B18	SSTL15
DQS0	E26	DIFF_SSTL15_T_DCI
xDQS0	F26	DIFF_SSTL15_T_DCI
DQS1	B27	DIFF_SSTL15_T_DCI
xDQS1	C27	DIFF_SSTL15_T_DCI
DQS2	C30	DIFF_SSTL15_T_DCI
xDQS2	D30	DIFF_SSTL15_T_DCI
DQS3	K18	DIFF_SSTL15_T_DCI
xDQS3	K17	DIFF_SSTL15_T_DCI
DQS4	M18	DIFF_SSTL15_T_DCI
xDQS4	M17	DIFF_SSTL15_T_DCI
DQS5	G15	DIFF_SSTL15_T_DCI
xDQS5	F15	DIFF_SSTL15_T_DCI
DQS6	G11	DIFF_SSTL15_T_DCI
xDQS6	F11	DIFF_SSTL15_T_DCI
DQS7	B12	DIFF_SSTL15_T_DCI
xDQS7	B13	DIFF_SSTL15_T_DCI
DM0	B26	SSTL15
DM1	H27	SSTL15
DM2	A31	SSTL15
DM3	E17	SSTL15
DM4	E16	SSTL15
DM5	M15	SSTL15
DM6	H14	SSTL15
DM7	J12	SSTL15
A0	F20	SSTL15
A1	A21	SSTL15
A2	A20	SSTL15
A3	E23	SSTL15
A4	E22	SSTL15
A5	B22	SSTL15
A6	B21	SSTL15
A7	J21	SSTL15
A8	F21	SSTL15
A9	J20	SSTL15
A10	B23	SSTL15
A11	G22	SSTL15
A12	G21	SSTL15
A13	A24	SSTL15
A14	A23	SSTL15

DDR2 Pin Name	FPGA	
	Pin No.	IO Standard
DQ0	C24	SSTL15_T_DCI
DQ1	A26	SSTL15_T_DCI
DQ2	A25	SSTL15_T_DCI
DQ3	B25	SSTL15_T_DCI
DQ4	D26	SSTL15_T_DCI
DQ5	D27	SSTL15_T_DCI
DQ6	C25	SSTL15_T_DCI
DQ7	D25	SSTL15_T_DCI
DQ8	D29	SSTL15_T_DCI
DQ9	G28	SSTL15_T_DCI
DQ10	D24	SSTL15_T_DCI
DQ11	E24	SSTL15_T_DCI
DQ12	G27	SSTL15_T_DCI
DQ13	B28	SSTL15_T_DCI
DQ14	G25	SSTL15_T_DCI
DQ15	G26	SSTL15_T_DCI
DQ16	H29	SSTL15_T_DCI
DQ17	H28	SSTL15_T_DCI
DQ18	A28	SSTL15_T_DCI
DQ19	A30	SSTL15_T_DCI
DQ20	B30	SSTL15_T_DCI
DQ21	B31	SSTL15_T_DCI
DQ22	F28	SSTL15_T_DCI
DQ23	A29	SSTL15_T_DCI
DQ24	L19	SSTL15_T_DCI
DQ25	D17	SSTL15_T_DCI
DQ26	G17	SSTL15_T_DCI
DQ27	H17	SSTL15_T_DCI
DQ28	E18	SSTL15_T_DCI
DQ29	F18	SSTL15_T_DCI
DQ30	B17	SSTL15_T_DCI
DQ31	C17	SSTL15_T_DCI
DQ32	K19	SSTL15_T_DCI
DQ33	J19	SSTL15_T_DCI
DQ34	H18	SSTL15_T_DCI
DQ35	L16	SSTL15_T_DCI
DQ36	L14	SSTL15_T_DCI
DQ37	B16	SSTL15_T_DCI
DQ38	F16	SSTL15_T_DCI
DQ39	G16	SSTL15_T_DCI
DQ40	M16	SSTL15_T_DCI
DQ41	J17	SSTL15_T_DCI

DDR2 Pin Name	FPGA	
	Pin No.	IO Standard
BA0	H20	SSTL15
BA1	G20	SSTL15
BA2	K21	SSTL15
CK0	B20	DIFF_SSTL15
xCK0	C19	DIFF_SSTL15
CK1	C20	DIFF_SSTL15
xCK1	D20	DIFF_SSTL15
CKE0	J22	SSTL15
CKE1	C23	SSTL15
xCS0	K22	SSTL15
xCS1	A18	SSTL15
xRAS	H19	SSTL15
xCAS	E19	SSTL15
xWE	D19	SSTL15
XRESET	H22	SSTL15
XEVENT	C18	SSTL15
SCL	L21	LVCMOS15
SDA	L20	LVCMOS15

DDR2 Pin Name	FPGA	
	Pin No.	IO Standard
DQ42	D15	SSTL15_T_DCI
DQ43	B15	SSTL15_T_DCI
DQ44	A15	SSTL15_T_DCI
DQ45	D16	SSTL15_T_DCI
DQ46	H15	SSTL15_T_DCI
DQ47	J15	SSTL15_T_DCI
DQ48	A14	SSTL15_T_DCI
DQ49	A13	SSTL15_T_DCI
DQ50	D14	SSTL15_T_DCI
DQ51	C14	SSTL15_T_DCI
DQ52	F14	SSTL15_T_DCI
DQ53	E14	SSTL15_T_DCI
DQ54	G12	SSTL15_T_DCI
DQ55	G13	SSTL15_T_DCI
DQ56	K14	SSTL15_T_DCI
DQ57	H12	SSTL15_T_DCI
DQ58	H10	SSTL15_T_DCI
DQ59	M13	SSTL15_T_DCI
DQ60	C12	SSTL15_T_DCI
DQ61	J14	SSTL15_T_DCI
DQ62	M11	SSTL15_T_DCI
DQ63	G10	SSTL15_T_DCI

7.7. PCI Express Edge

The board provides one PCI Express Edge interface (CN2). It can be linked as x1, x4, x8 Gen2.
The PCI Express interface is on PCIE-FPGA (U48).
Table 7-11 shows the edge pin assign of the PCI Express Edge.

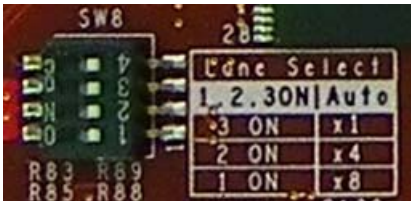
Table 7-11 PCI Express Edge Pinout Table

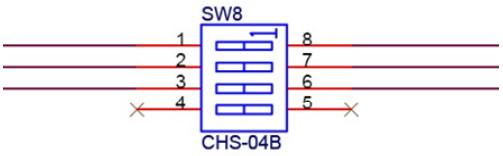
Bank No.	Pin No.	A		B	Pin No.	Bank No.
		*1 PRSNT1#	1	*2 +12V		
		*2 +12V	2	*2 +12V		
		*2 +12V	3	*2 +12V		
		GND	4	GND		
		*3 JTAG_TCK	5	*3 SMCLK		
		*3 JTAG_TDI	6	*3 SMDAT		
		*3 JTAG_TDO	7	GND		
		*3 JTAG_TMS	8	*2 +3.3V		
		*2 +3.3V	9	JTAG1_TRST#		
		*2 +3.3V	10	*2 +3.3VAUX		
24	R16	PERST#	11	*3 WAKE#		

Bank No.	Pin No.	A		B	Pin No.	Bank No.
KEY						
		GND	12	*3 RSVD		
MGTREFCLK0P_115	L4	REFCLK+	13	GND		
MGTREFCLK0N_115	L3	REFCLK-	14	PETP0	B1	MGTRXP3_115
		GND	15	PETN0	B2	MGTRXN3_115
MGTTXP3_115	D1	PERP0	16	GND		
MGTTXN3_115	D2	PERN0	17	*1 PRSNT2#		
		GND	18	GND		
		*3 RSVD	19	PETP1	C3	MGTRXP2_115
		GND	20	PETN1	C4	MGTRXN2_115
MGTTXP2_115	F1	PERP1	21	GND		
MGTTXN2_115	F2	PERN1	22	GND		
		GND	23	PETP2	E3	MGTRXP1_115
		GND	24	PETN2	E4	MGTRXN1_115
MGTTXP1_115	H1	PERP2	25	GND		
MGTTXN1_115	H2	PERN2	26	GND		
		GND	27	PETP3	G3	MGTRXP0_115
		GND	28	PETN3	G4	MGTRXN0_115
MGTTXP0_115	K1	PERP3	29	GND		
MGTTXN0_115	K2	PERN3	30	*3 RSVD		
		GND	31	*1 PRSNT2#		
		*3 RSVD	32	GND		
		*3 RSVD	33	PETP4	W3	MGTRXP3_114
		GND	34	PETN4	W4	MGTRXN3_114
MGTTXP3_114	M1	PERP4	35	GND		
MGTTXN3_114	M2	PERN4	36	GND		
		GND	37	PETP5	Y1	MGTRXP2_114
		GND	38	PETN5	Y2	MGTRXN2_114
MGTTXP2_114	P1	PERP5	39	GND		
MGTTXN2_114	P2	PERN5	40	GND		
		GND	41	PETP6	AA3	MGTRXP1_114
		GND	42	PETN6	AA4	MGTRXN1_114
MGTTXP1_114	T1	PERP6	43	GND		
MGTTXN1_114	T2	PERN6	44	GND		
		GND	45	PETP7	AB1	MGTRXP0_114
		GND	46	PETN7	AB2	MGTRXN0_114
MGTTXP0_114	V1	PERP7	47	GND		
MGTTXN0_114	V2	PERN7	48	*1 PRSNT2#		
		GND	49	GND		

*** 1 PRSNT1#, PRSNT2#**

The signals are used for Hot-plug detection. Please refer to PCI Express specification. Figure 7-14 and Table 7-12 show the setting of PRSNT pins.





Lane Select	
1,2,3ON	auto select
1ON	x8
2ON	x4
3ON	x1

Figure 7-14 PRSNT# Setting Structure

Table 7-12 PCI Express Lane Setting Table

Device	Pin No.	Function	Note
SW8	1	x8	Default = ON
	2	x4	Default = ON
	3	x1	Default = ON
	4	Unused	

*** 2 Power supply**

Power can be supply to the board from the PCI Express edge. But they are unused in this design.

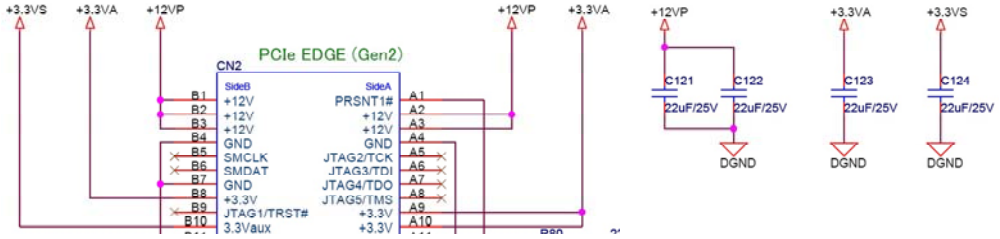


Figure 7-15 Power Supply from PCIE Edge

*** 3 TCK, TMS, TDI, TDO, TRST#, WAKE#, RSVD**

They are unused in this design.

7.8. Analog Connector

The board provides a 4 input/4 output port analog connector. And there are 4 sets analog input and 4 sets analog output circuit on the board.
Table 7-13 shows the feature of the analog part.

Table 7-13 Feature of Analog Part

Analog Input	
Number of Inputs	4 Channel Single End
Resolution	16 bit
Sampling Rate	250KS/s
Input Voltage	±5V
Used Device	AD7689BCPZ
Analog Output	
Number of Outputs	4 Channel Single End
Resolution	16 bit
Output Voltage	±5V or +5V
Used Device	AD5754RBREZ

Table 7-14 shows the pinout of the analog connector.

Table 7-14 Analog Connector Pinout Table

Device		Analog Connector				Device	
Ref No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Ref No.
U34	3	AIN_0	1	2	AIN_1	3	U31
U30	3	AIN_2	3	4	AIN_3	3	U28
		GND	5	6	GND		
U40	1	AOUT_0	7	8	AOUT_1	7	U40
U38	1	AOUT_2	9	10	AOUT_3	7	U38
		GND	11	12	GND		

7.9. Digital Connector

The board provides a 4 input/4 output port digital connector to user FPGA (U46).
Table 7-15 shows the pinout of the digital connector.

Table 7-15 Digital Connector Pinout Table

FPGA		Digital Connector				FPGA	
Bank No.	Pin No.	Pin Name	Pin No.	Pin No.	Pin Name	Pin No.	Bank No.
35	E12	DI0	1	2	DO0	E13	35
35	A11	DI1	3	4	DO1	F13	35
35	B11	DI2	5	6	DO2	D12	35
35	J11	DI3	7	8	DO3	C13	35
		GND	9	10	3P3V		

7.10. USB (UART)

The board provides a Mini-Type USB interface connector (CN9) as a means to communicate with an external device, using the USB-RS232C conversion device (U42) for UART communication with FPGA (U46).

Table 7-16 UART Pinout Table

Signal Name	USER FPGA (U46)		
	Pin No.	Bank	Level
CP2103_RXD	AB26	13	2.5V
CP2103_TXD	AG32	13	
CP2103_CTS	AA26	13	
CP2103_RTS	AG33	13	

7.11. LED

The board provides 8 onboard LEDs. These LEDs will light when Low is output from FPGA.

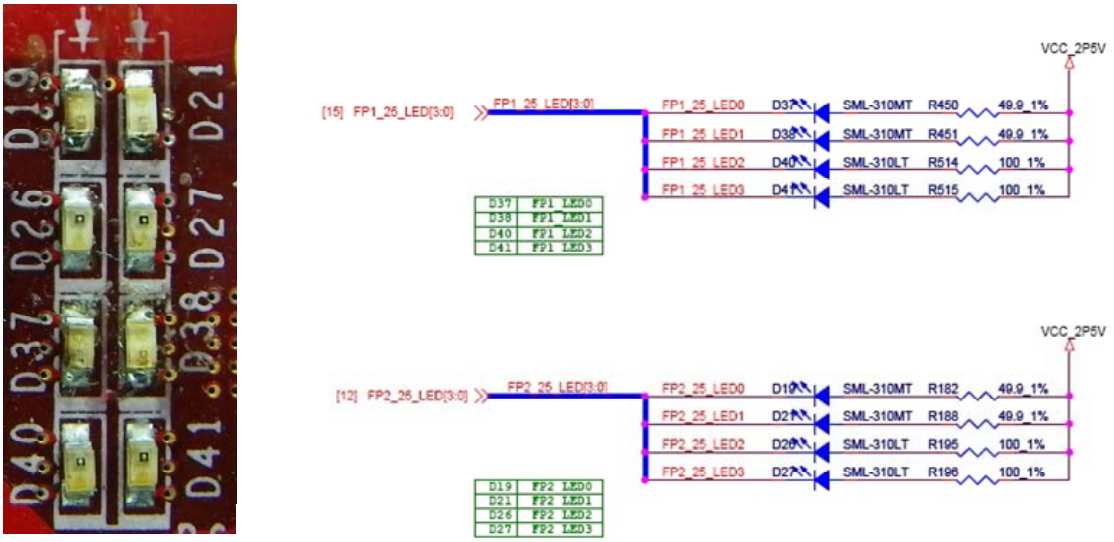


Figure 7-16 LED Structure

Table 7-17 LED Pinout Table

Device		FPGA			
Name	Signal Name	FPGA No.	Pin No.	Bank	Level
D37	FP1_LED0	USER(U46)	F23	24	2.5V
D38	FP1_LED1		F24	24	
D40	FP1_LED2		L24	24	
D41	FP1_LED3		M23	24	
D19	FP2_LED0	PCIE(U48)	AA9	34	
D21	FP2_LED1		Y9	34	
D26	FP2_LED2		V10	34	
D27	FP2_LED3		U9	34	

7.12. DIPSW

The board provides three 4 pole DIPSWs. When the DIPSW is set to the ON side, it generates Low output on the associated FPGA pin.

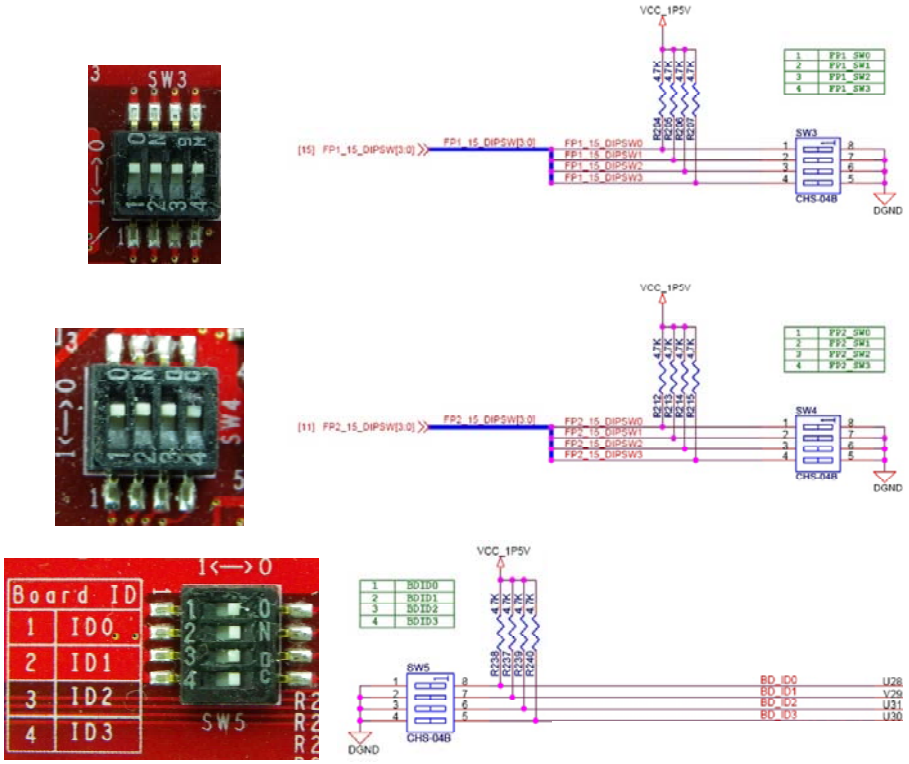


Figure 7-17 DIPSW Structure

Table 7-18 DIPSW Pinout Table

Device		FPGA			
Name	Signal Name	FPGA No.	Pin No.	Bank	Level
SW3	FP1_15_DIPSW0	USER(U46)	W26	14	1.5V
	FP1_15_DIPSW1		W27	14	
	FP1_15_DIPSW2		V25	14	
	FP1_15_DIPSW3		W25	14	
SW4	FP2_15_DIPSW0	PCIE(U48)	F7	35	1.5V
	FP2_15_DIPSW1		G8	35	
	FP2_15_DIPSW2		H8	35	
	FP2_15_DIPSW3		C12	35	
SW5	BD_ID0	PCIE(U48)	U28	14	1.5V
	BD_ID1		V29	14	
	BD_ID2		U31	14	
	BD_ID3		U30	14	

7.13. PushSW

The board provides 2 function PushSWs. When the PushSW is held down, it generates Low output on the associated FPGA pin.

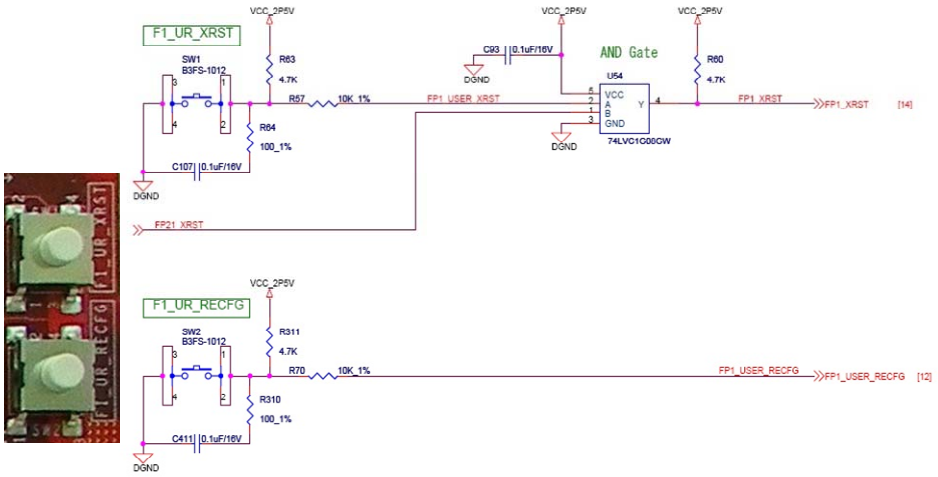


Figure 7-18 PushSW Structure

Table 7-19 PushSW Pinout Table

Device		FPGA			
Name	Signal Name	Device No.	Pin No.	Bank	Level
SW1	FP1_USER_XRST	U46	AF34	13	2.5V
SW2	FP1_USER_RECFG	U48	T17	24	

7.14. Slide SW

The board provides 5 slide-switches to select the impedance of the external signal and the program chain of the FPGA. The 3 of 5 switches are used for selecting the FPGA program chain. The others are used for setting the impedance of the external signals.

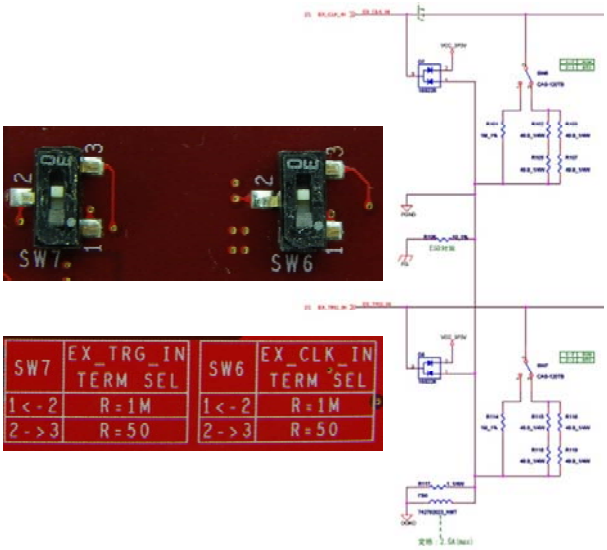


Figure 7-19 Impedance Selection of External Signal

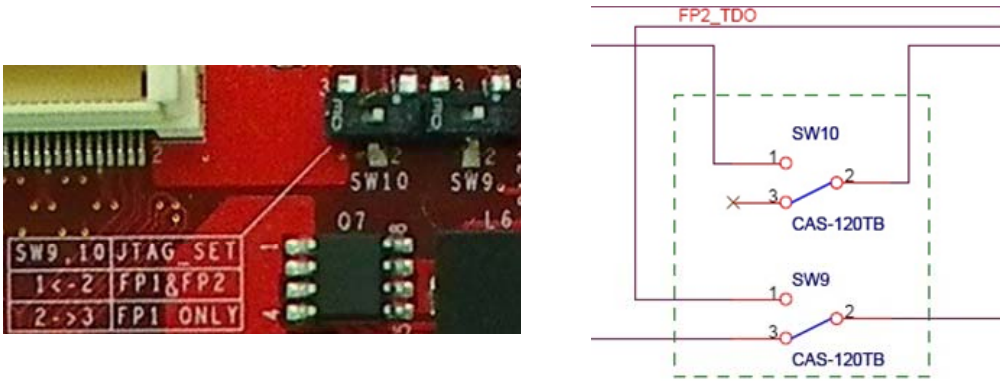


Figure 7-20 Program Chain Selection

7.15. External Power Supply Connector

The board provides an external power supply connectors.

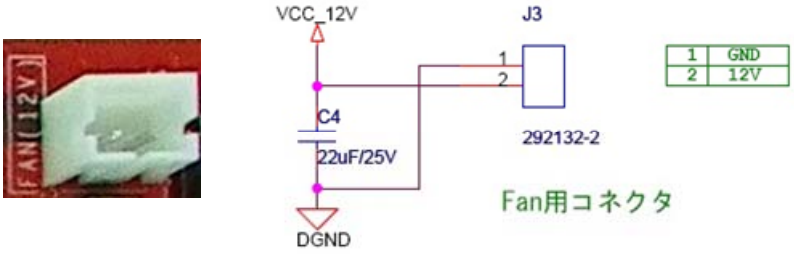


Figure 7-21 External Power Supply Connector Structure

Table 7-20 External Power Supply Connector Pinout Table

Type	No.	# of Pin	Pin 1	Pin 2
FAN Connector	J3	2pin	GND	12V

7.16. Battery Control

The board provides the battery control (soldering side) connected to the VBATT (T5) pin of the PCIE FPGA and VBATT (N8) pin of the User FPGA. Use a CR1220 button battery. This socket is not inserted at factory.

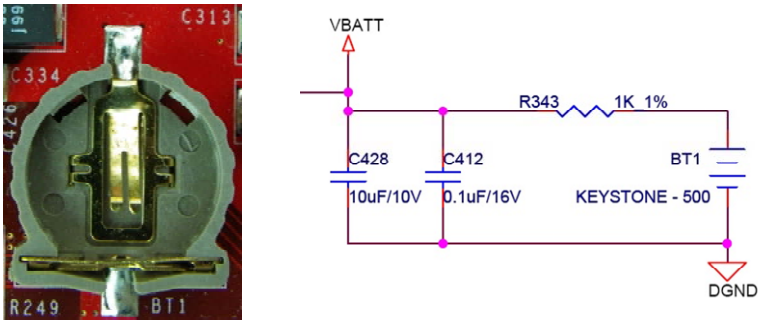


Figure 7-22 Battery Structure

8. Appendix

8.1. Creating a Configuration File

This section describes how to create a configuration file.
Tool is ISE 11.4.

Create a configuration file to write into the Flash memory.

1. Double-click ISE Tool

iMPACT..
2. Click **No**

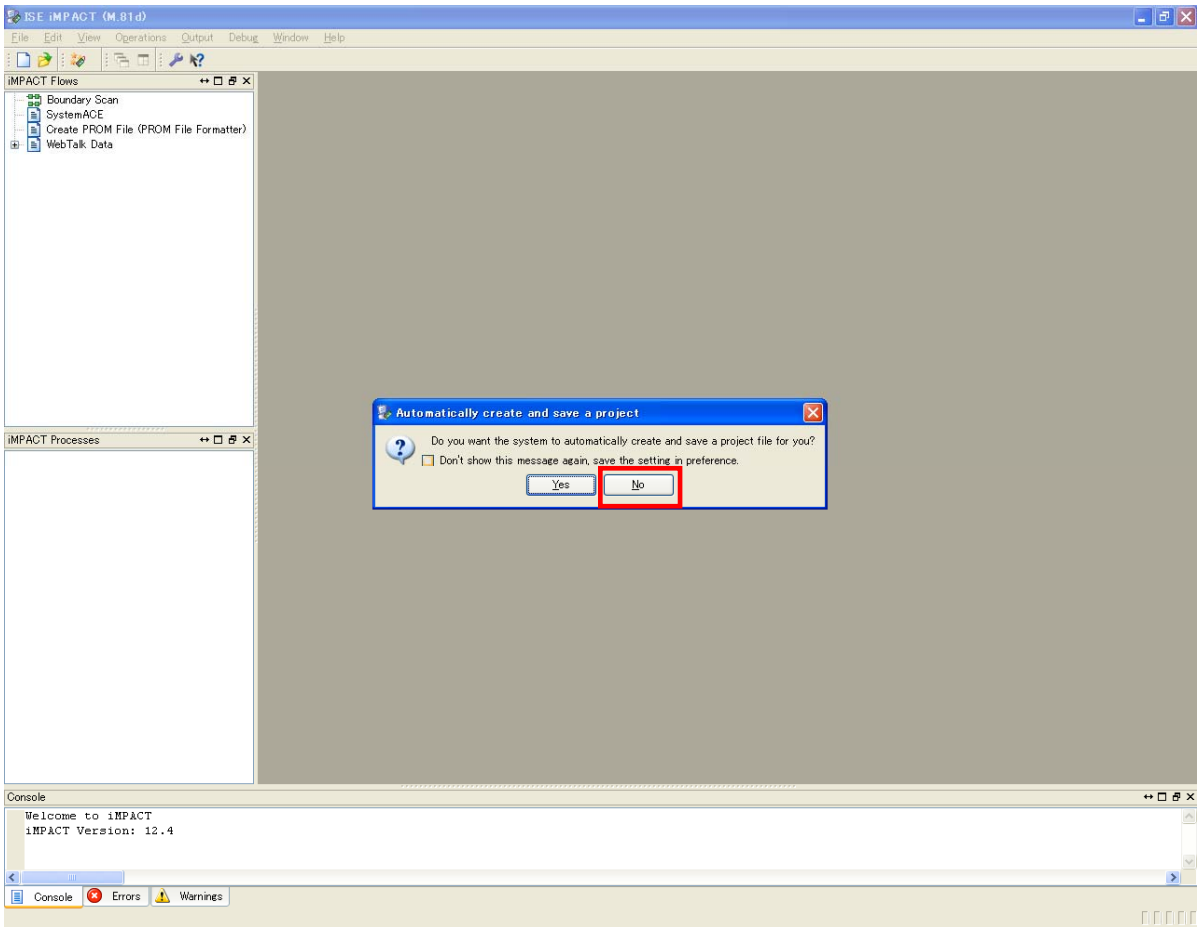


Figure8-1 iMPACT Window 1

3. Choose **Cancel**

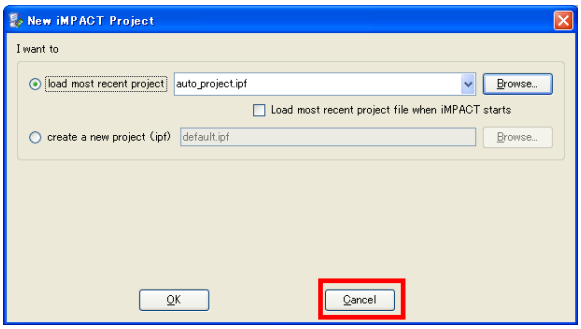


Figure8-2 iMPACT Window 2

4. Double-click **Create PROM File (PROM File Formatter)**.

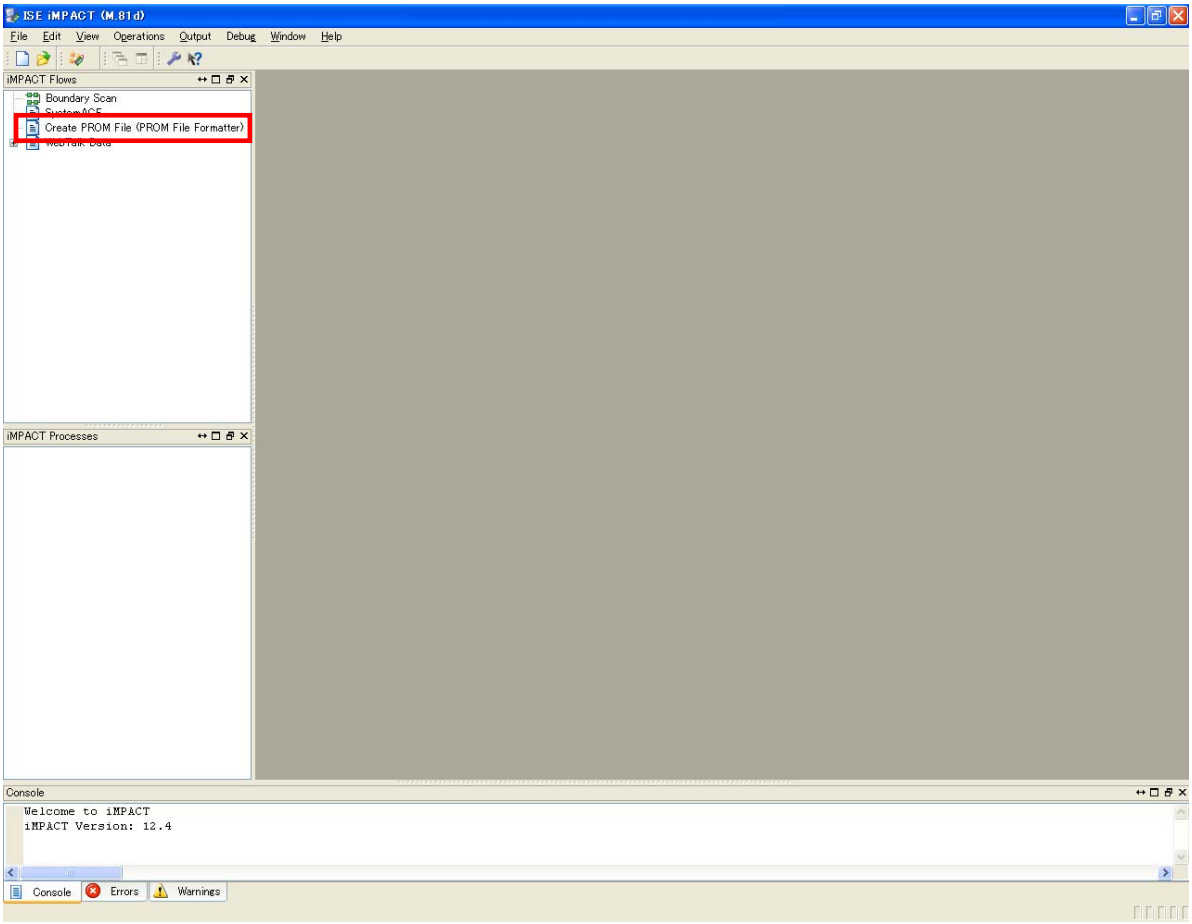


Figure8-3 iMPACT Window 3

5. Choose **BPI Flash - Configure Single FPGA** and then click the right-pointing arrow.

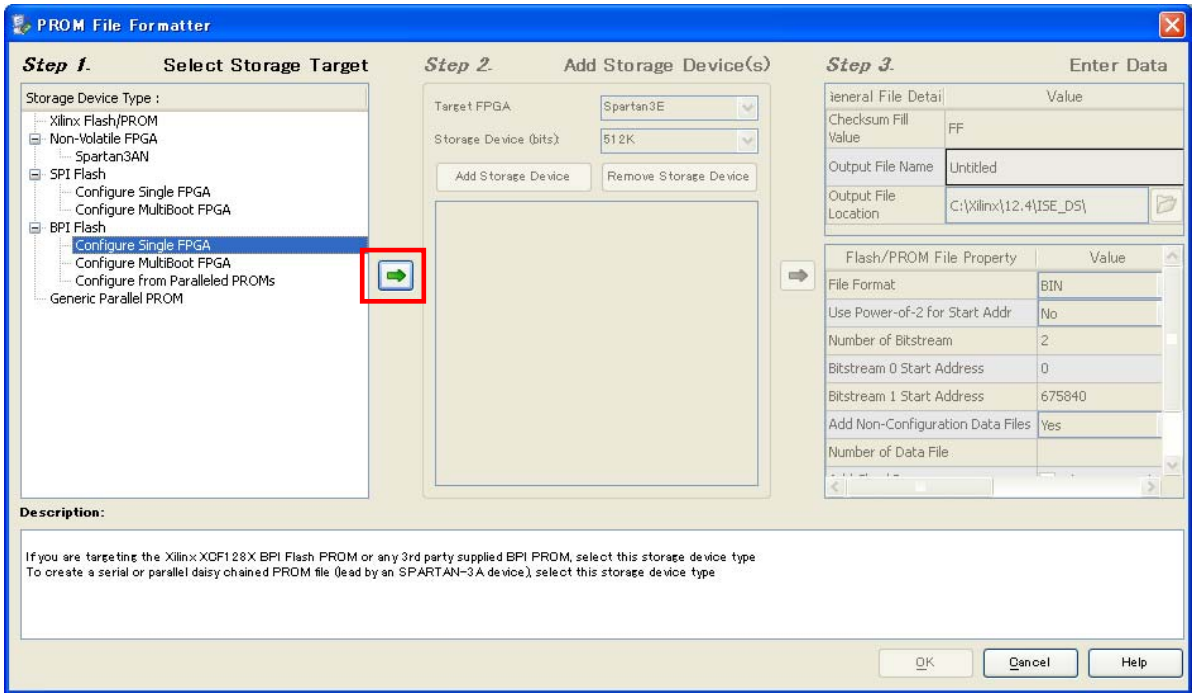


Figure8-4 iMPACT Window 4

6. On Storage Device (bits) select **Viretex6** and **128M,** and then click **Add Storage Device**.

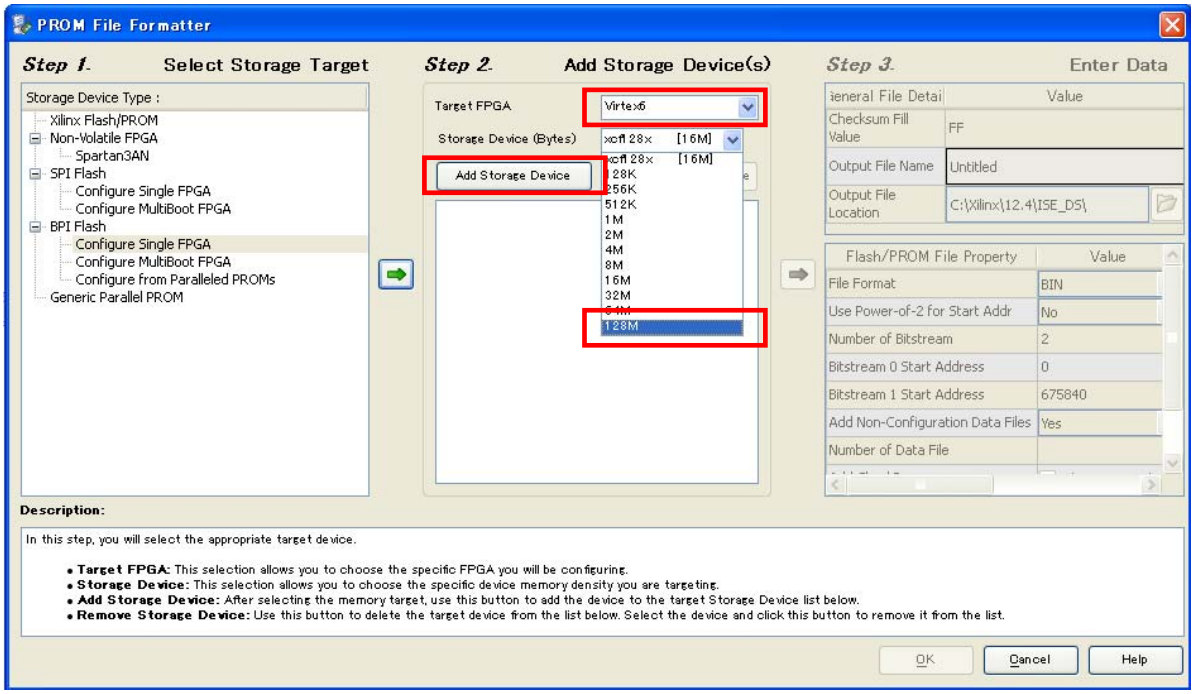


Figure8-5 iMPACT Window 5

7. Click the right-pointing arrow. Enter a name of directory and location in the **Output File Name** and **Output File Location** fields and then click **OK**.

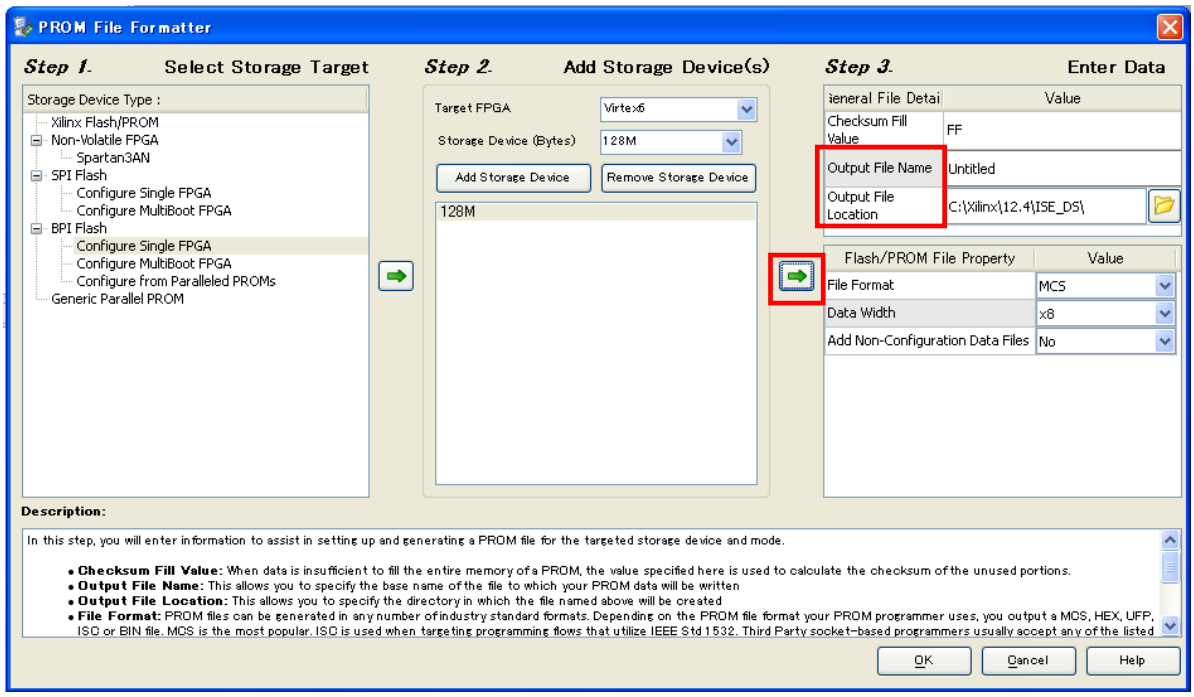

PROM File Formatter
Step 1. Select Storage Target
Storage Device Type :
Xilinx Flash/PROM
Non-Volatile FPGA
Spartan3AN
SPI Flash
Configure Single FPGA
Configure MultiBoot FPGA
BPI Flash
Configure Single FPGA
Configure MultiBoot FPGA
Configure from Paralleled PROMs
Generic Parallel PROM
Step 2. Add Storage Device(s)
Target FPGA
Virtex6
Storage Device (Bytes)
128M
Add Storage Device
Remove Storage Device
128M
Step 3. Enter Data
ieneral File Detai
Value
Checksum Fill Value
FF
Output File Name
Untitled
Output File Location
C:\Xilinx\12.4\ISE_DS\
Flash/PROM File Property
Value
File Format
MCS
Data Width
x8
Add Non-Configuration Data Files
No
Description:
In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.
Checksum Fill Value: When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
Output File Name: This allows you to specify the base name of the file to which your PROM data will be written
Output File Location: This allows you to specify the directory in which the file named above will be created
File Format: PROM files can be generated in any number of industry standard formats. Depending on the PROM file format your PROM programmer uses, you output a MCS, HEX, UFP, ISC or BIN file. MCS is the most popular. ISC is used when targeting programming flows that utilize IEEE Std 1532. Third Party socket-based programmers usually accept any of the listed
OK
Cancel
Help

Figure8-6 iMPACT Window 6

8. Click **OK**.

Figure8-7 iMPACT Window 7

9. Select a bit file to create a configuration file.

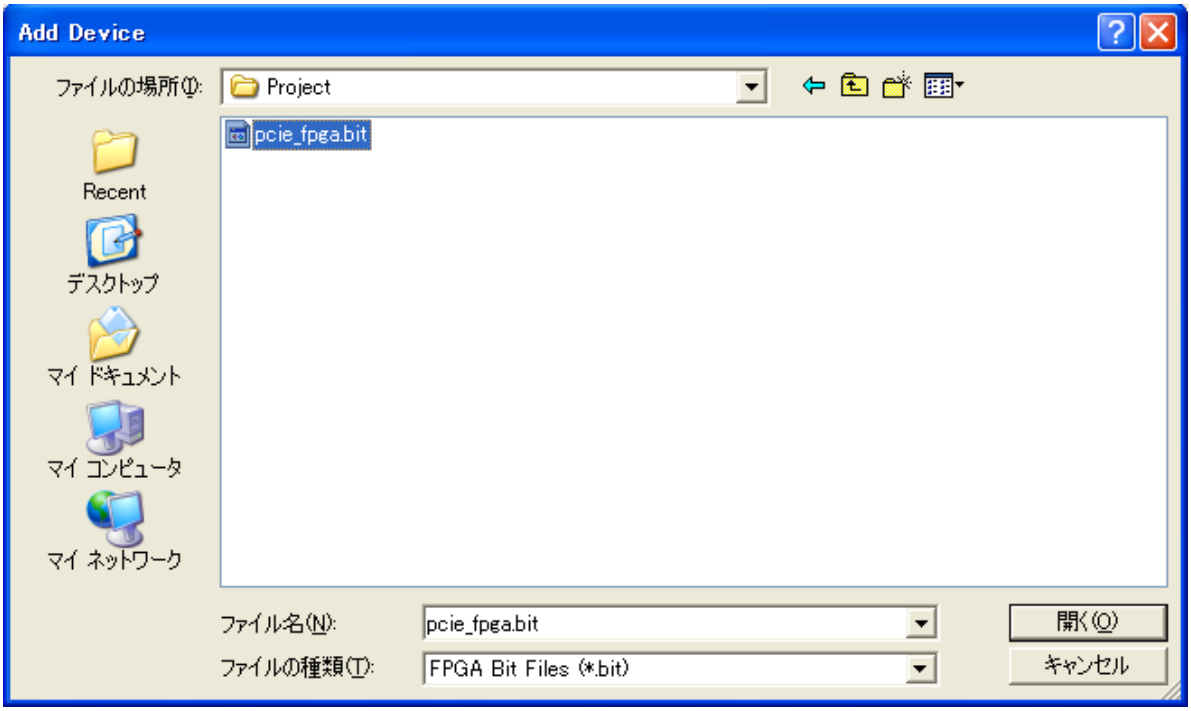


Figure8-8 iMPACT Window 8

10. Click **No**.

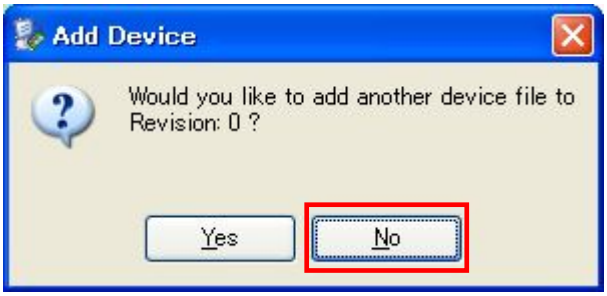


Figure8-9 iMPACT Window 9

11. Click **OK**.

Figure8-10 iMPACT Window 10

12. Click **OK**.

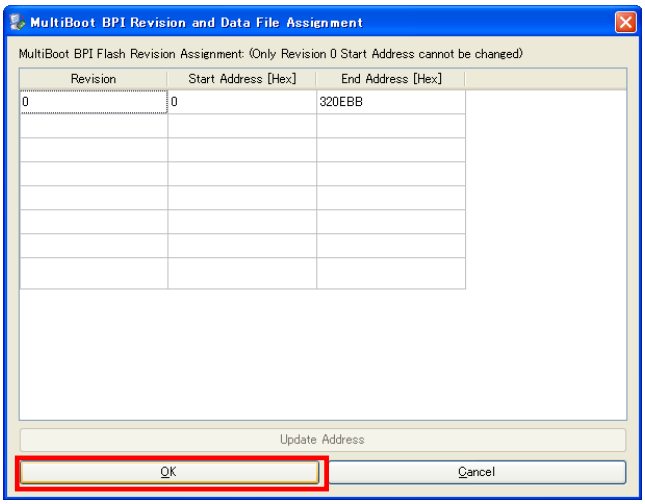


Figure8-11 iMPACT Window 11

13. Double-click **Generate File**.

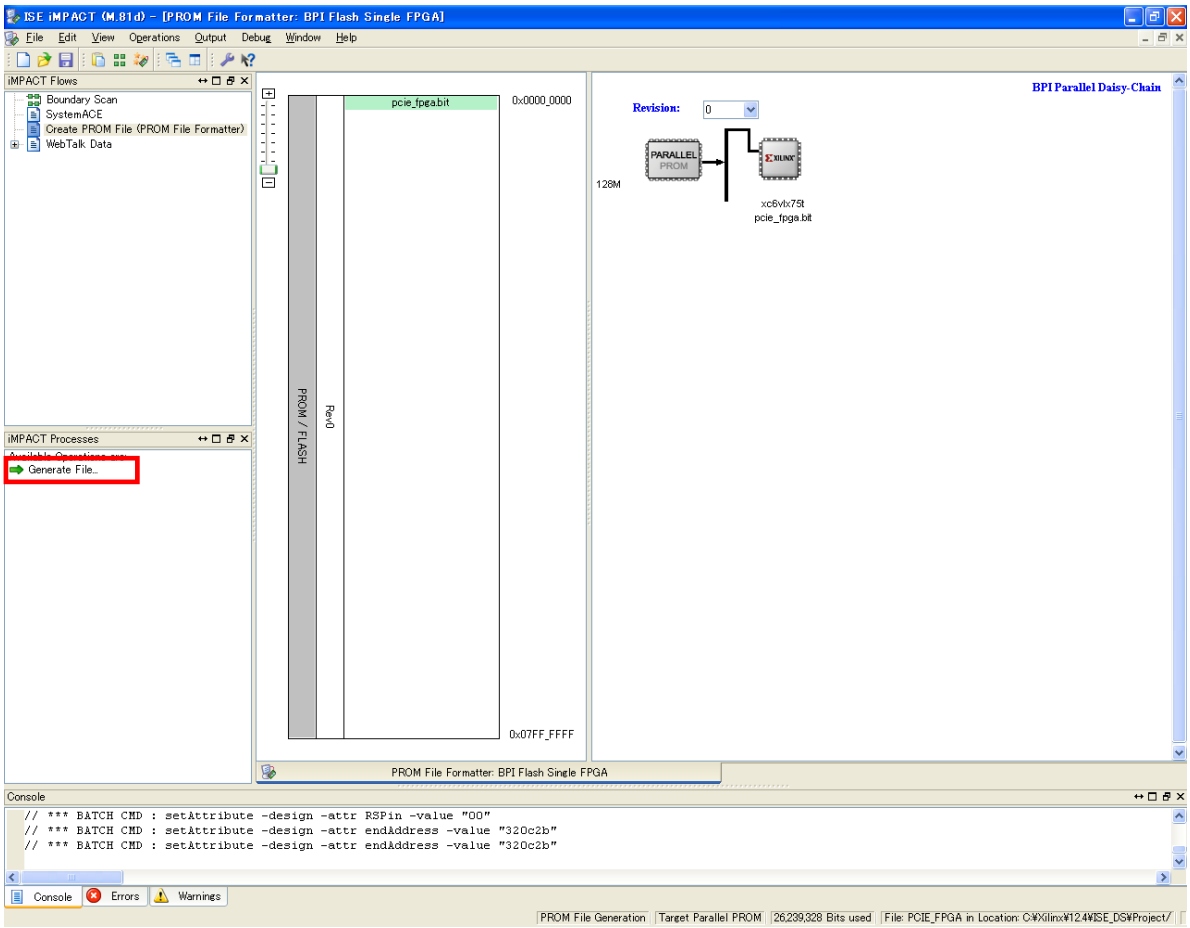


Figure8-12 iMPACT Window 12

14. If the configuration file has been successfully created, a message **PROM File Generation Succeeded** will appear.

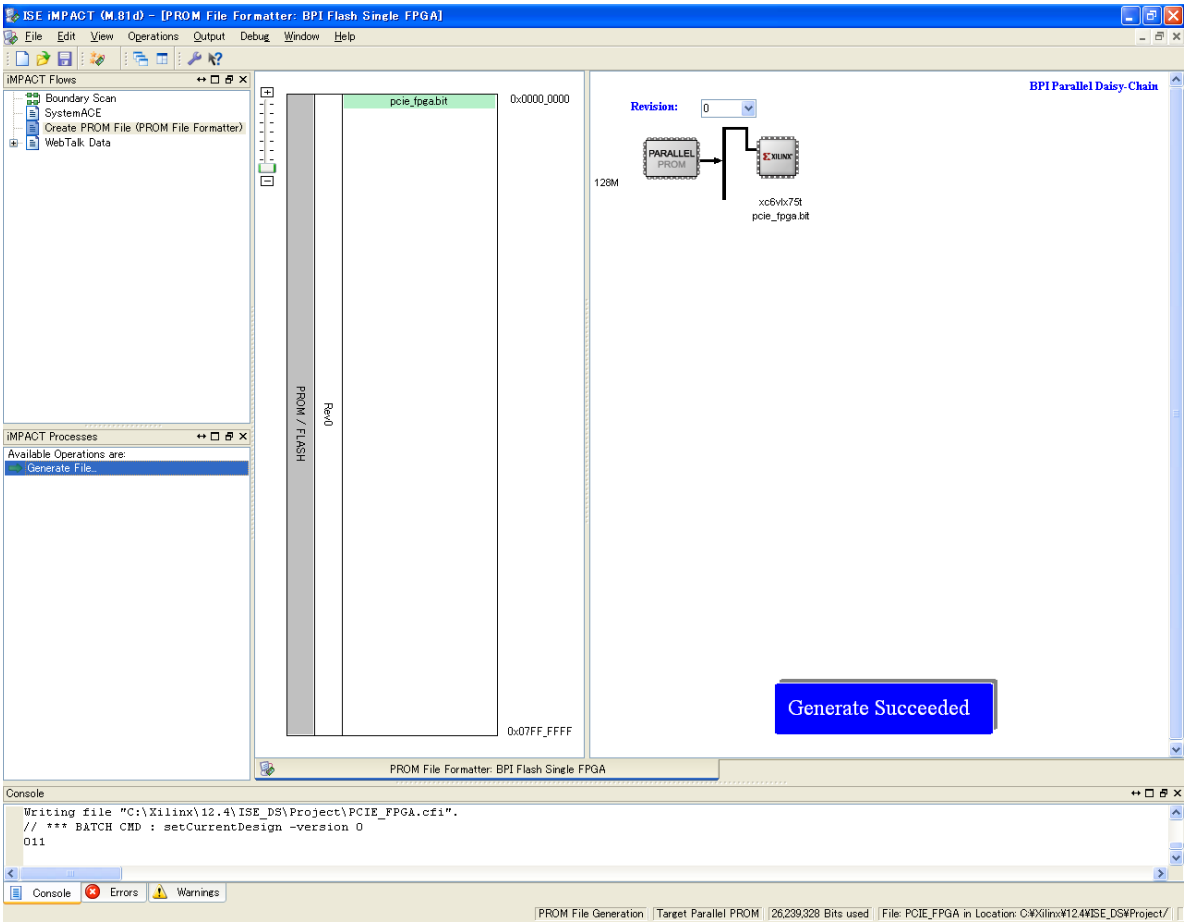


Figure8-13 iMPACT Window 13

8.2. Writing a Configuration File into the Flash Memory

Connect a Platform USB cable to the JTAG connector (CN11) as shown in Figure 8-xx. After powering on the board, start the iMPACT and write a configuration file into the Flash memory following the procedure described below.

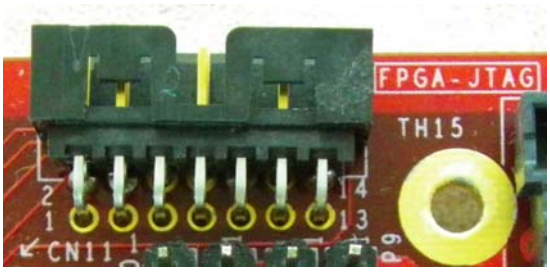


Figure8-14 Onboard JTAG Connector

1. Double-click **Boundary Scan** and then click **Initialize Chain** shown by the arrow.

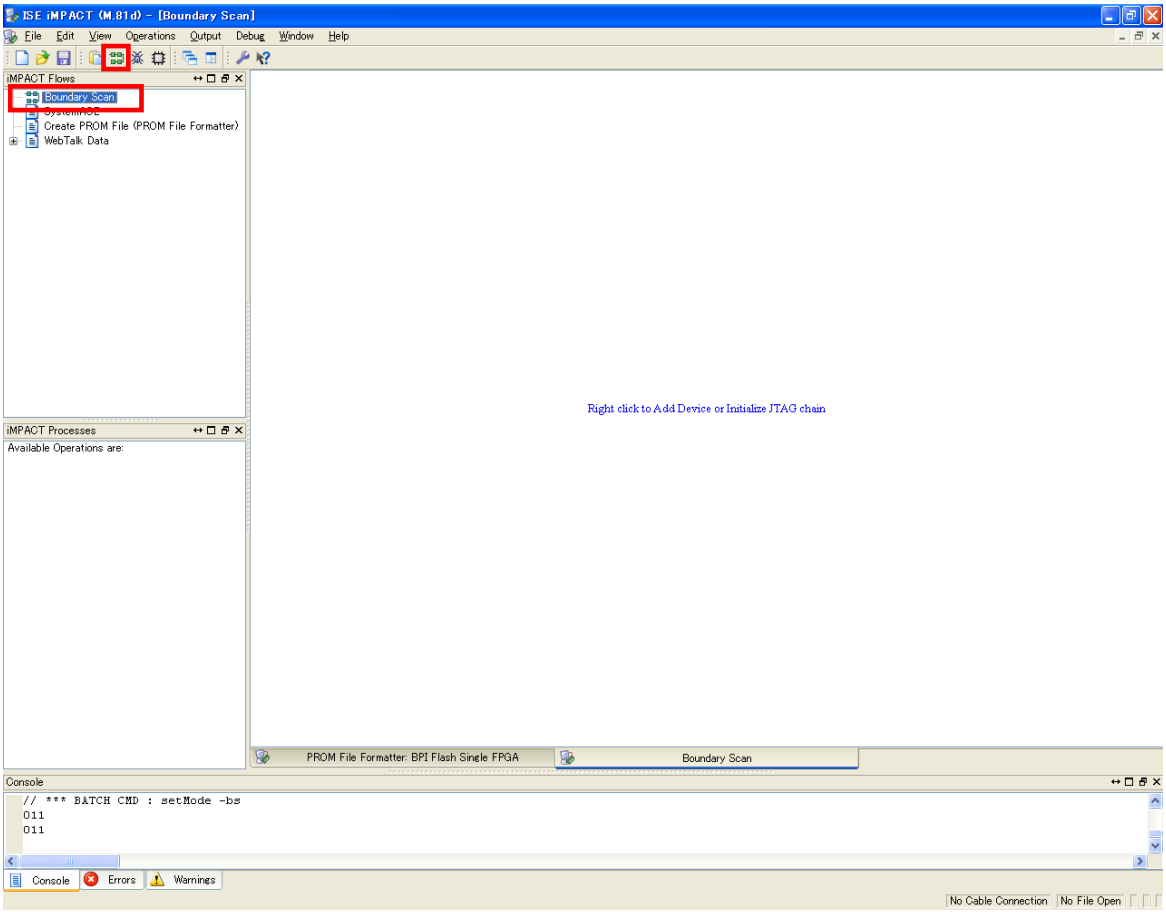


Figure8-15 Writing into the Device 1

2. Click **No**.

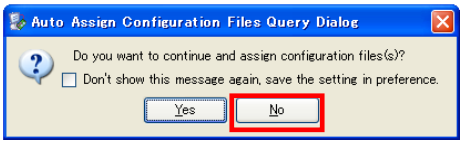

Auto Assign Configuration Files Query Dialog
Do you want to continue and assign configuration files(s)?
Don't show this message again, save the setting in preference.
Yes
No

Figure8-16 Writing into the Device 2

3. A bit/jed file configuration window will appear. Cancel it.
Select an FPGA and right-click to select **Add SPI/BPI Flash…**.

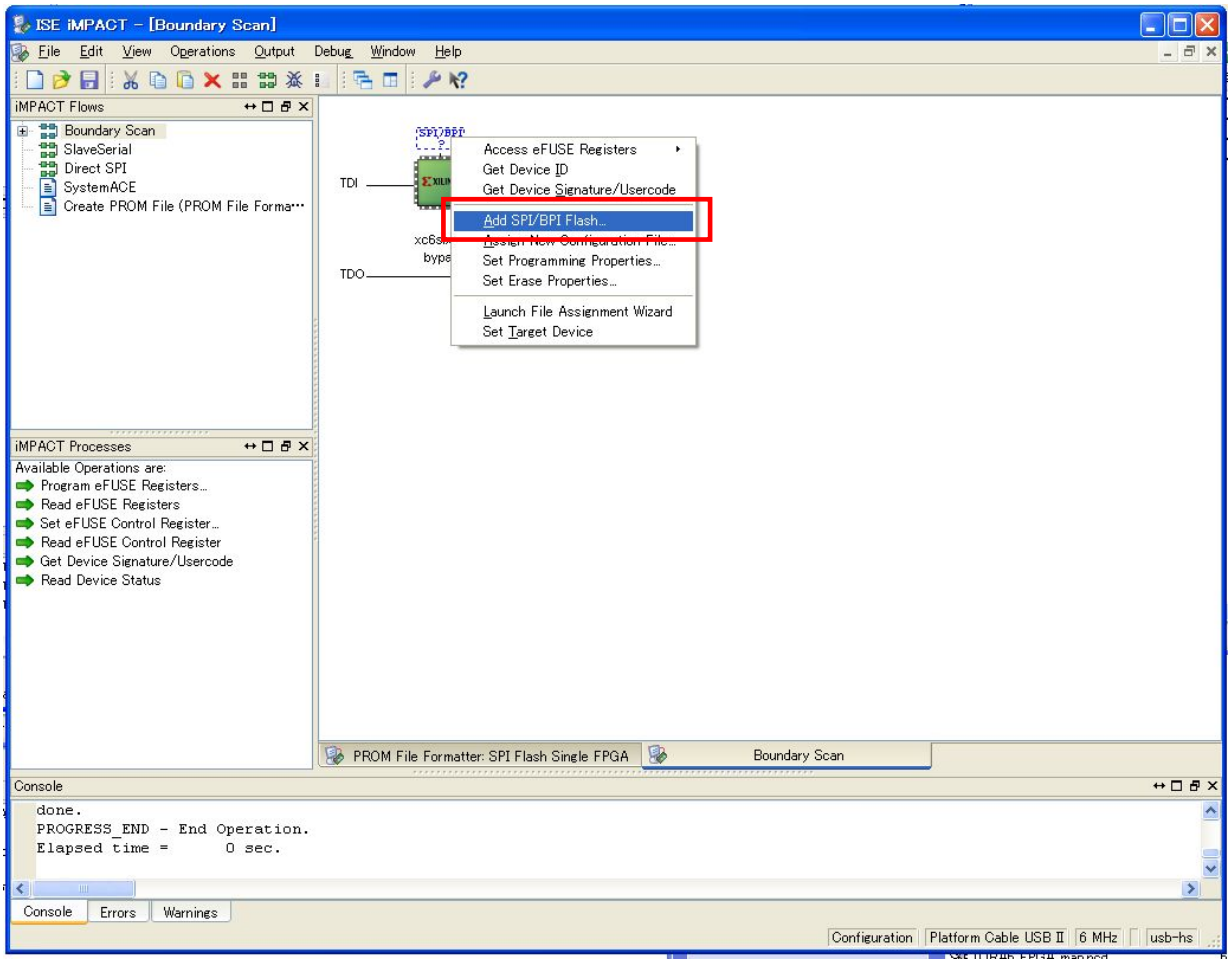


Figure8-17 Writing into the Device 2

3. Select a configuration file (xxx.mcs) to write into the Flash memory.

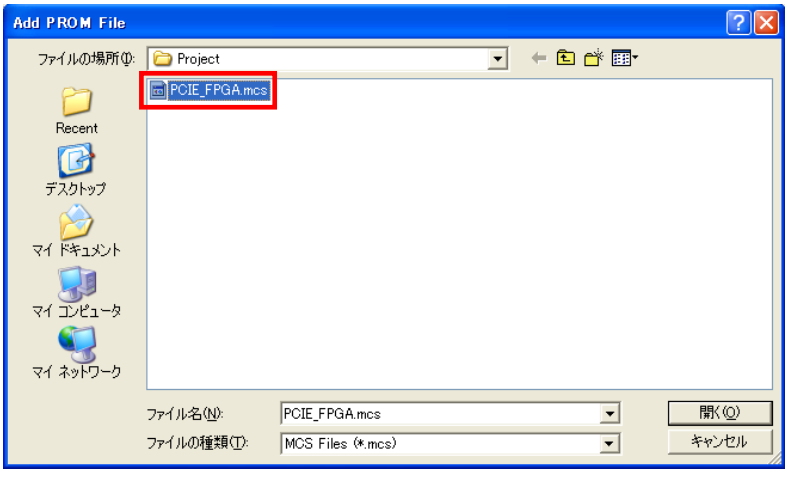


Figure8-18 Writing into the Device 3

4. Select the onboard Flash **SPANSIONS29GL128P** and click **OK**.

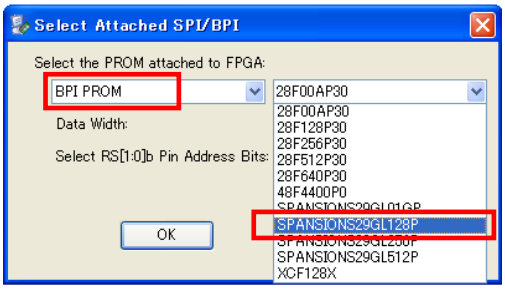


Figure8-19 Writing into the Device 4

5. On the **iMPACT Processes** window double-click **Program**.

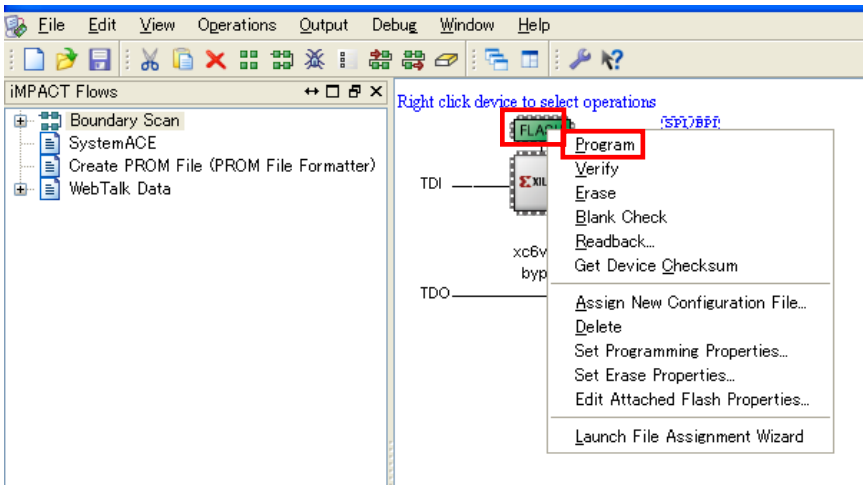


Figure8-20 Writing into the Device 5

6. Click **OK**.

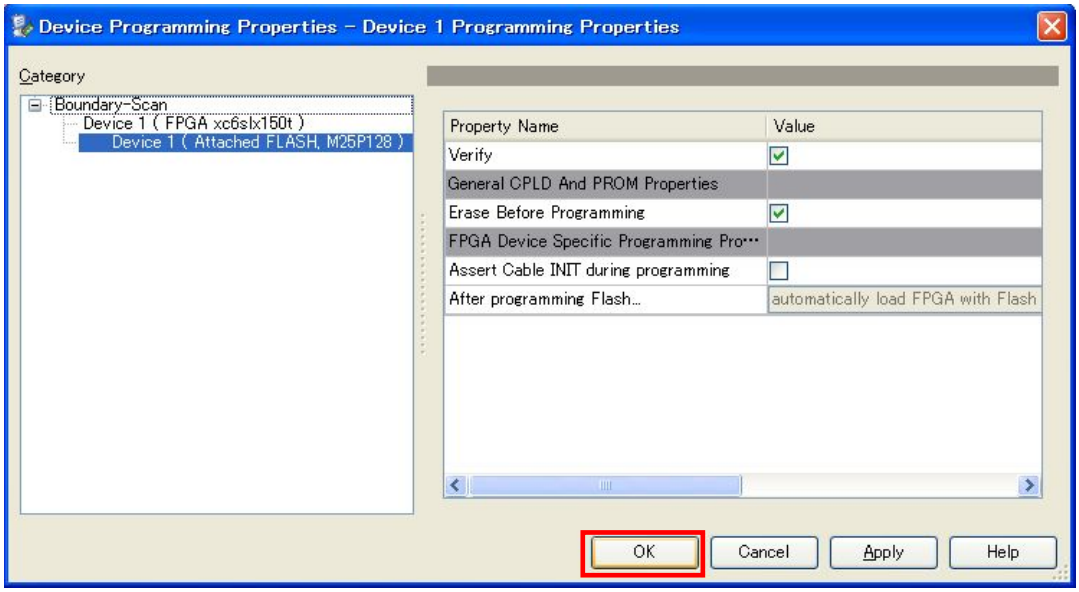


Figure8-21 Writing into the Device 6

7. The write operation into the Flash memory will start.

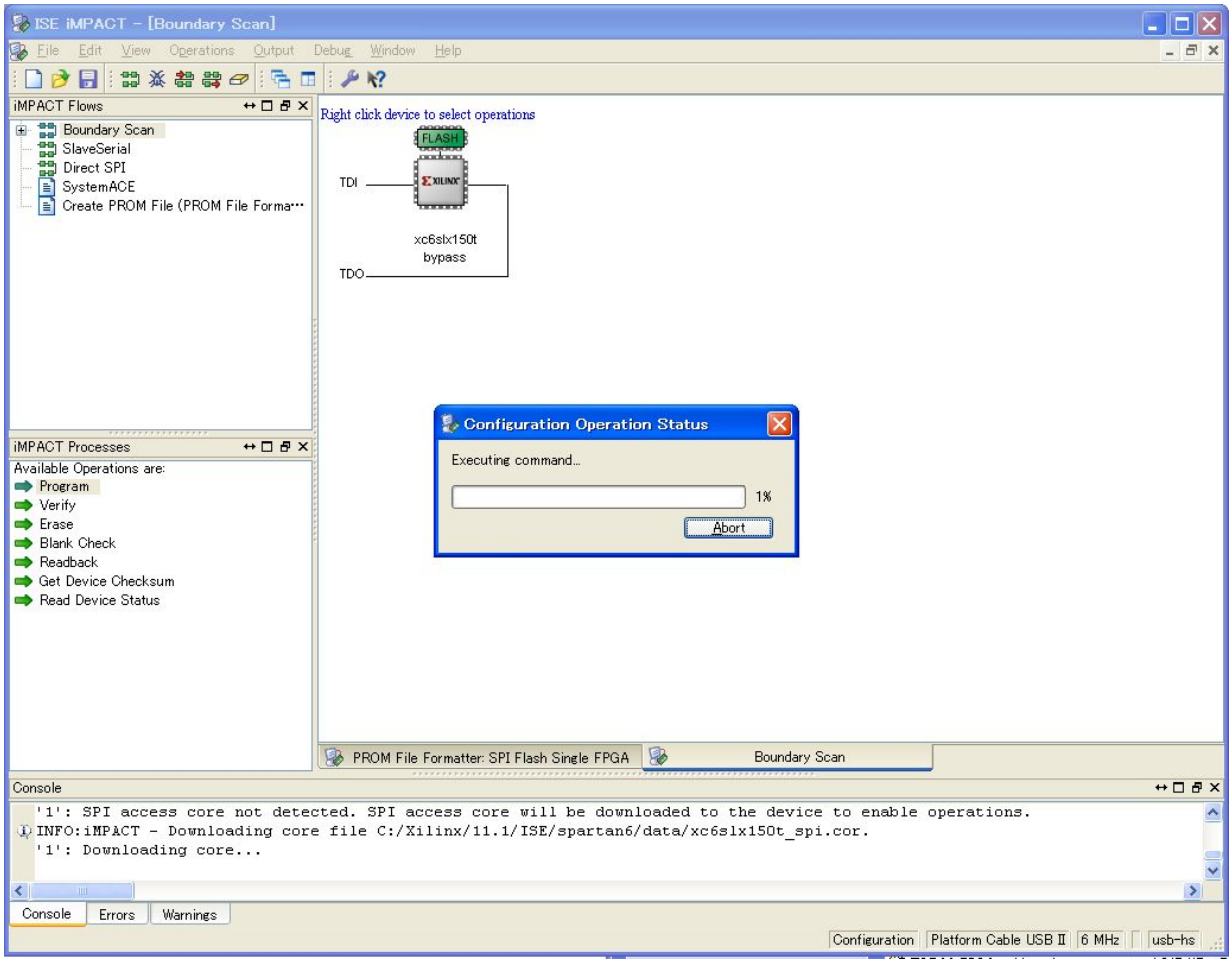


Figure8-22 Write into the Device 7

8. If the write operation into the Flash memory is successfully completed, a message **Program Succeeded** will appear.

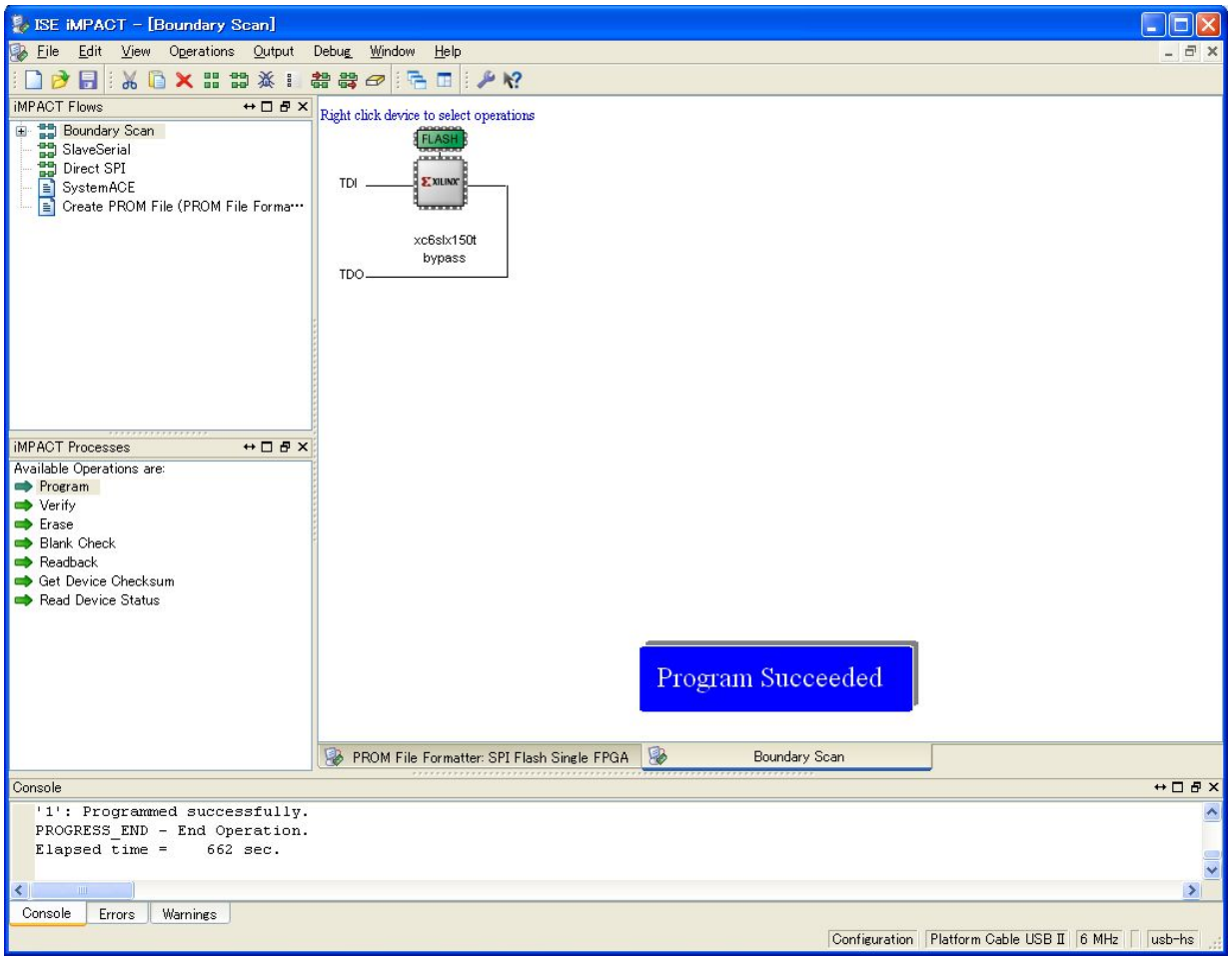


Figure8-23 Write into the Device 8

9. The data written in the Flash memory device is used for FPGA configuration using Master-SPI. The FPGA configuration can be initiated either by turning on the power switch of the board.

10. The board provides a LED (D34) for configuration status monitoring.
Green D34 indicates that the configuration process has been successfully completed.

8.3. Configuration Time

Time required to load configuration data into the Flash memory device can be changed by setting the configuration clock on ISE Tool.
Due to the operational frequency of BPI-Flash, select 16MHz or below.

Method:

1. Right-click **Generate Programming File**
2. Choose **Process Properties**
3. Choose **Configuration Options**
4. Change the **Value** of **Configuration Rate**.
   Configuration Clock Frequency (MHz) Setting

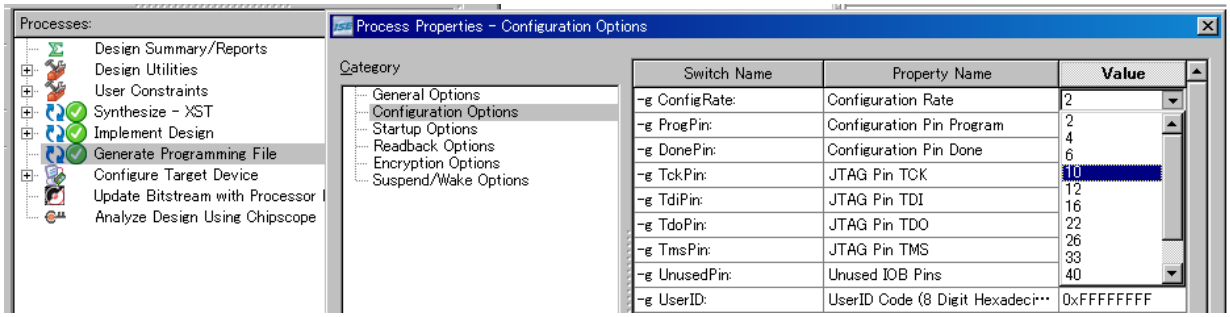


Figure 8-24 Changing Configuration Time

Target for Configuration Time:

Configuration Rate = 2MHz: Configuration Time = approx. 17 seconds
Configuration Rate = 10MHz: Configuration Time = approx. 6 seconds

9. Default Switch Settings

9.1. Figure 9-1 shows the default switch settings.

See the switches enclosed in blue box.

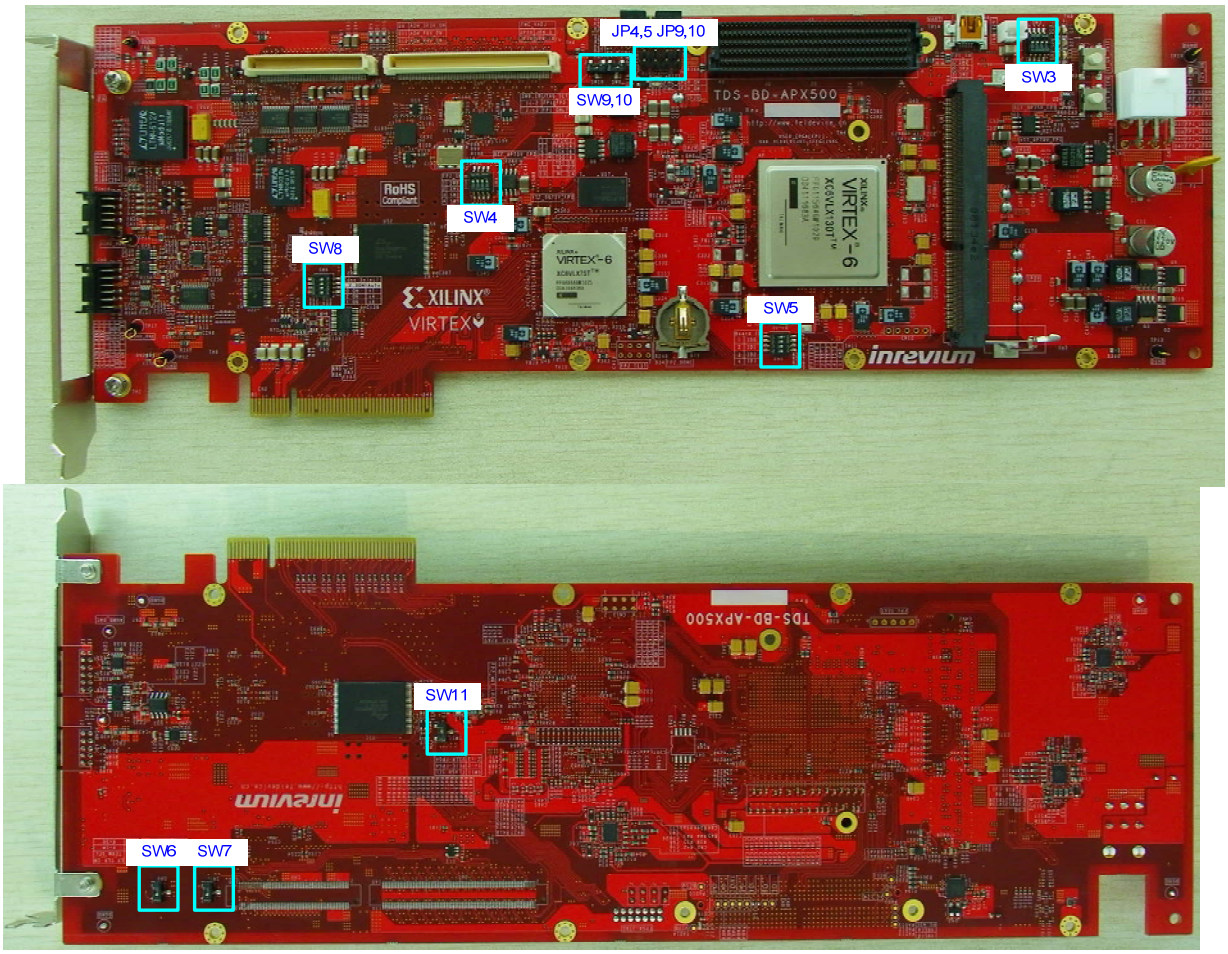


Figure9-1 Default Settings (component side)

Table 9-1 Default Settings

No.	Silk No.	Initial Setting	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			

TOKYO ELECTRON DEVICE

PLD Solution Division
URL: **http://www.inrevium.jp/eng/x-fpga-board/**
E-mail: psd-support@teldevice.co.jp

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